# Packaging of MEMS:
# an experience on LTCC

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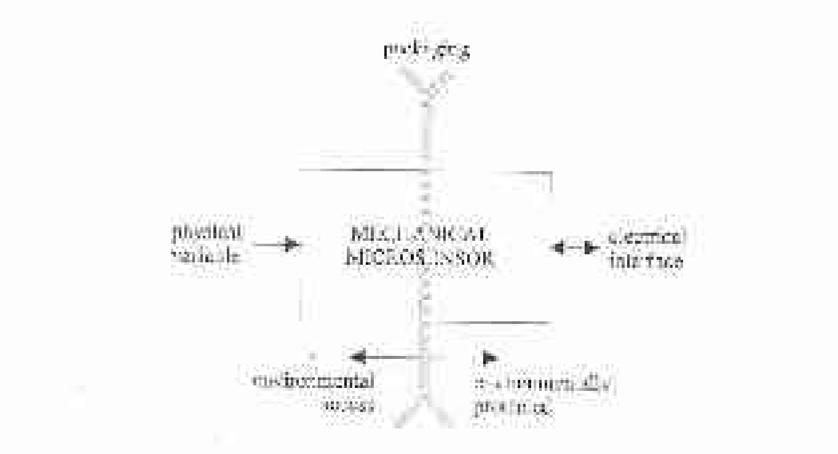
# Outline

- Introduction
- Functions and types of MEMS Packages
- Case studies
  - Microactuator on a LTCC packaging
  - RFID in a LTCC packaging
- Conclusions and work in progress

# Packaging of microelectronic

- Goal of the package:
  - to protect the chip from all outside influence
  - to provide electrical connection
  - to provide a heat flow path
- Single package type for different types of chips
- Detailed function of the chip is not important
- Package standards have been developed

# Packaging of MEMS



- Detailed function of the MEMS chip is critical to the design of the package
- MEMS and package have to be designed at the same time
- Difficult to develop standard package

# Functions of MEMS Packages

- Mechanical Support
  - thermal and mechanical shock
  - vibration
  - high acceleration
  - particles, etc.

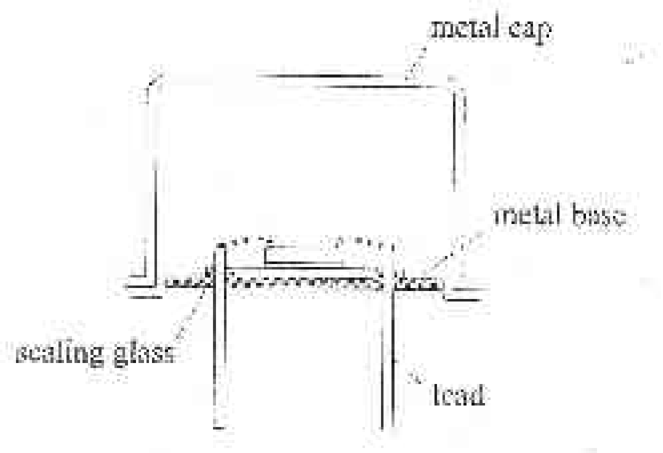
$CTE_{pack} \sim CTE_{Si}$ → die cracking
delamination

- Environmental contact
  - Protection from Environmental
    - corrosion & physical damage → "hermetic" packages
  - Environmental access

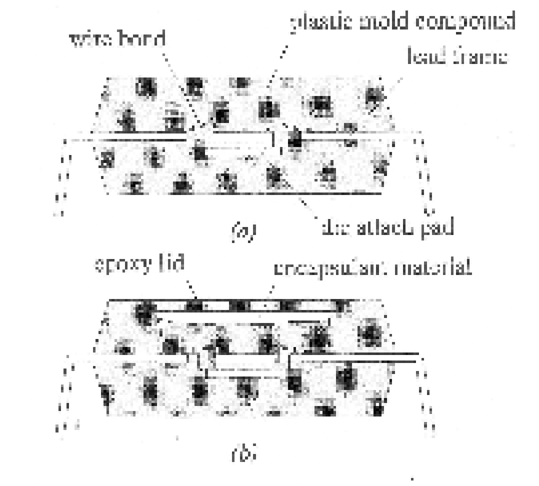
- Electrical Connection to other System Components
  - transfer DC and RF signals

# Types of MEMS Packages

- Metal Packages
  - - Excellent thermal dissipation
  - - Excellent electromagnetic shielding
  - - Excellent hermetic sealing



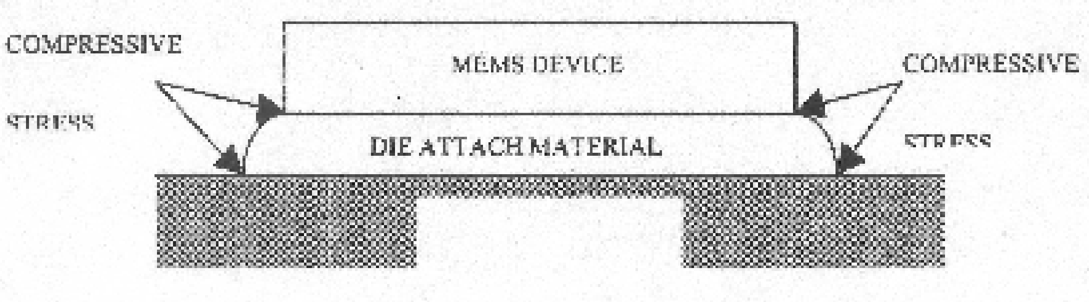
# Types of MEMS Packages



- Plastic Packages
  - No hermetic
  - Susceptible to cracking
- Ceramic Packages
  - Low mass
  - Low cost
  - Hermetic
  - Integrate signal distribution lines
  - Tailored package

# Package-to-MEMS Attachment

Differences on CTE cause thermomechanical stresses between MEMS silicon, attach material and package base



Solder bonging
Epoxy bonding
Glass bonding

# Case Studies

- Motivation
  - Set up of a MEMS packaging facility at INTI

Systems in a package

↓

Integration of MEMS and buried components in the same package

# Case Studies

- Microactuator on a LTCC packaging

- RFID in a LTCC packaging

# Why LTCC Packaging

- Ease of 3D multi-layers: Z dimension becomes part of the system
- Tapes are soft: pliable and easily machined (cavities structures)
- 3D curved structures
- Adaptability to embedded fluidic structures
- Communication between layers by vias (both fluidic and electronic)

# Why LTCC Packaging

- Support multiple assembly techniques: Solder (SMD & FC), Eutectic Welding, Wire Bond
- Integration of IC and MEMS
- Good match CTE between Si & LTCC

(2.6 ppm/°C vs 5 to 7 ppm/°C)

- Dielectric coefficient: 4.0 – 9.5
- Support multiple I/O (electrical, mechanical, optical, fluidic, gaseous, waveguide, thermal)

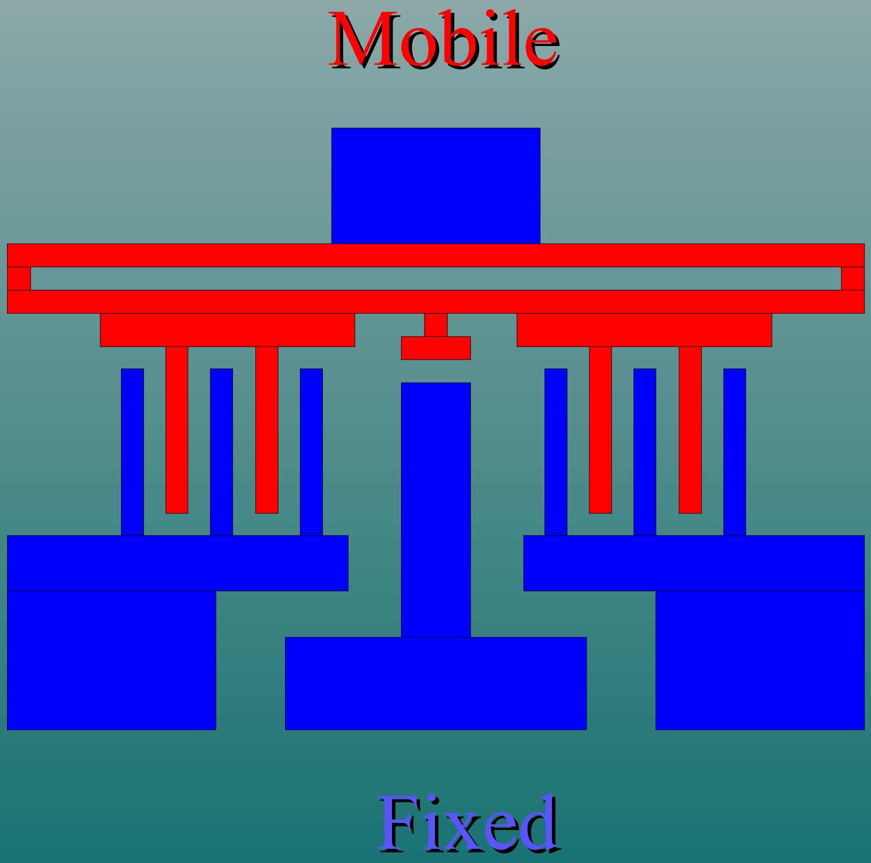
# Process Flow

- Design of packaging
- Selection of the materials
- Masks design
- Fabrication of package
- Assembly of prototypes

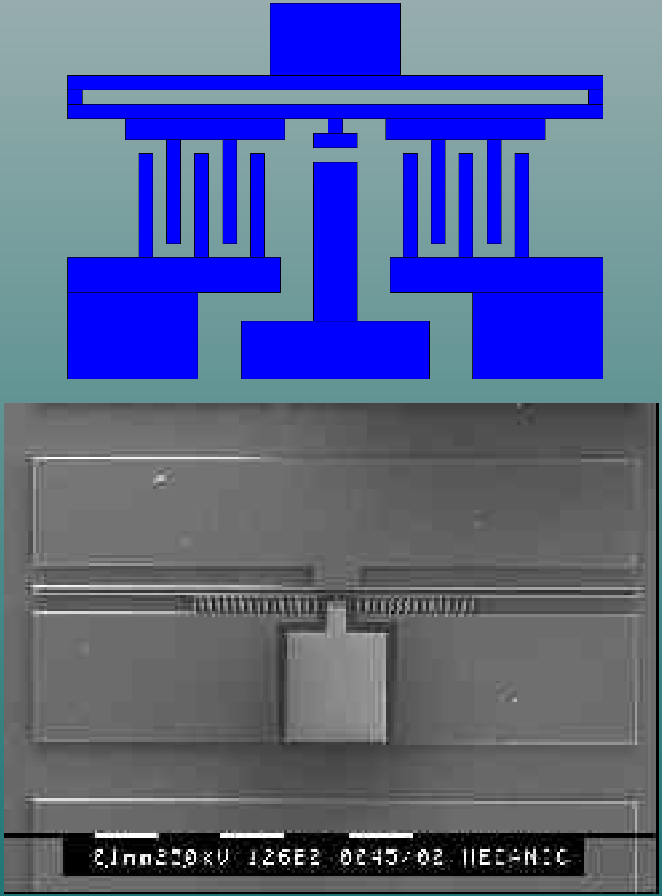
# Case Study I:
# Microactuator structure

Comb drive electrostatic actuator

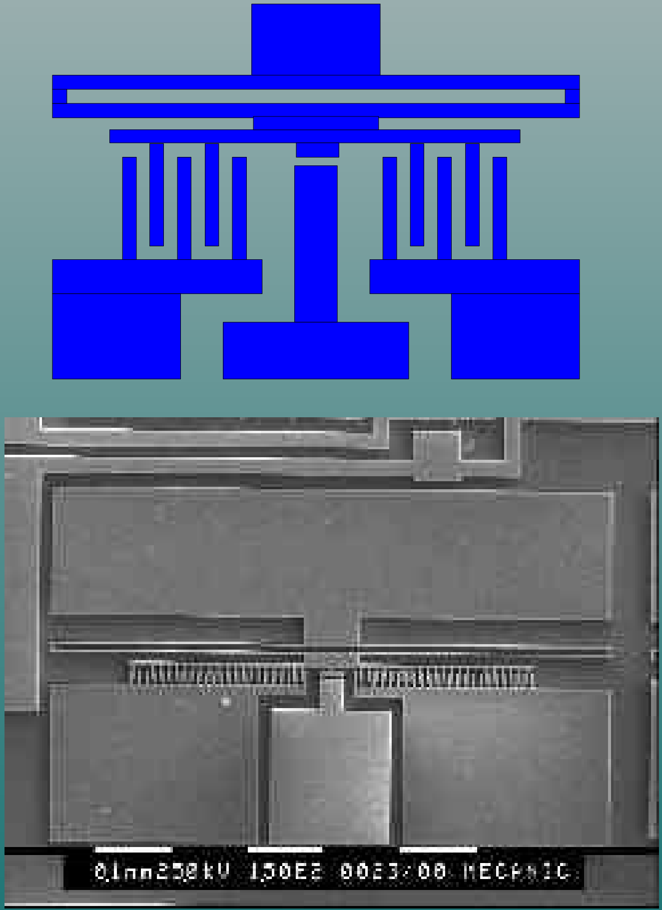
- Double-fold spring
- Pair of comb drives
- Moveable lateral contact



# Two basic structures

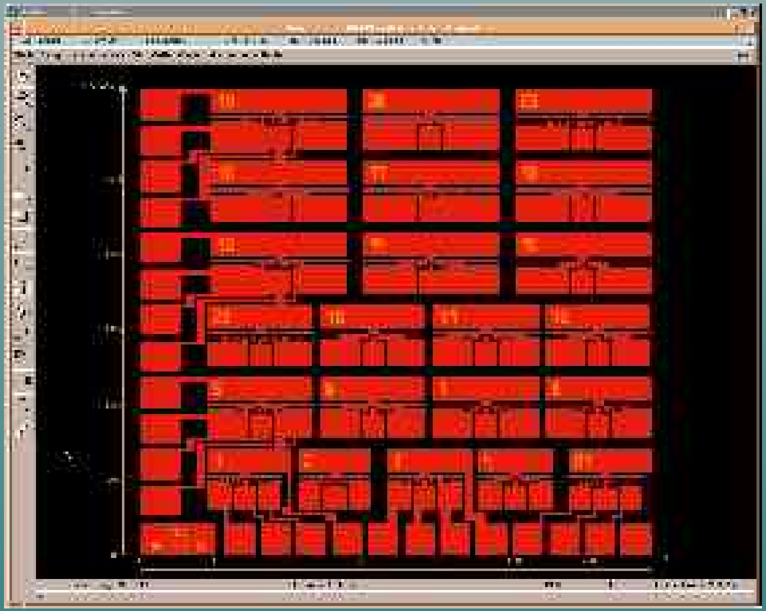


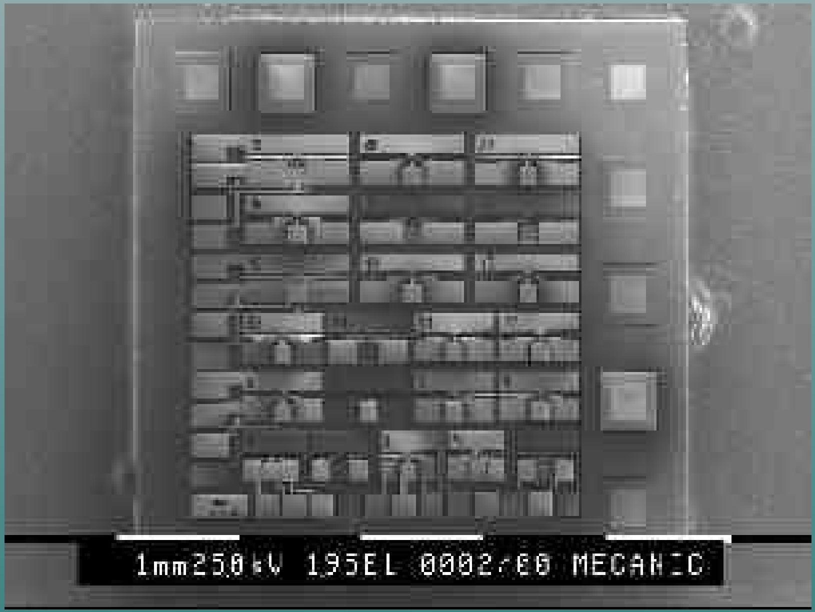
First design



Improvement of spring elasticity

# Microactuator Prototypes





Die size

4900 x 4600 µm

Active area

3400 x 3100 µm

Interconnection pads

Size: 200 x 200 µm

Pitch: 240 µm

# Package Design

Two models were proposed for multilayer packaging:

- Top contact design
  All electrical connections at one side of the packaging
- Bottom contact design
  Using vias

# Packaging dimensions

| | |
|---|---|
| Die´s cavity [mm$^2$] | 8x8 |
| Connection´s cavity [mm$^2$] | 14x14 |
| Internal pads [μm$^2$] | 400x800 |
| Internal pads pitch [μm$^2$] | 750 |
| Connection width [μm] | 200 |

Dimensions for both designs

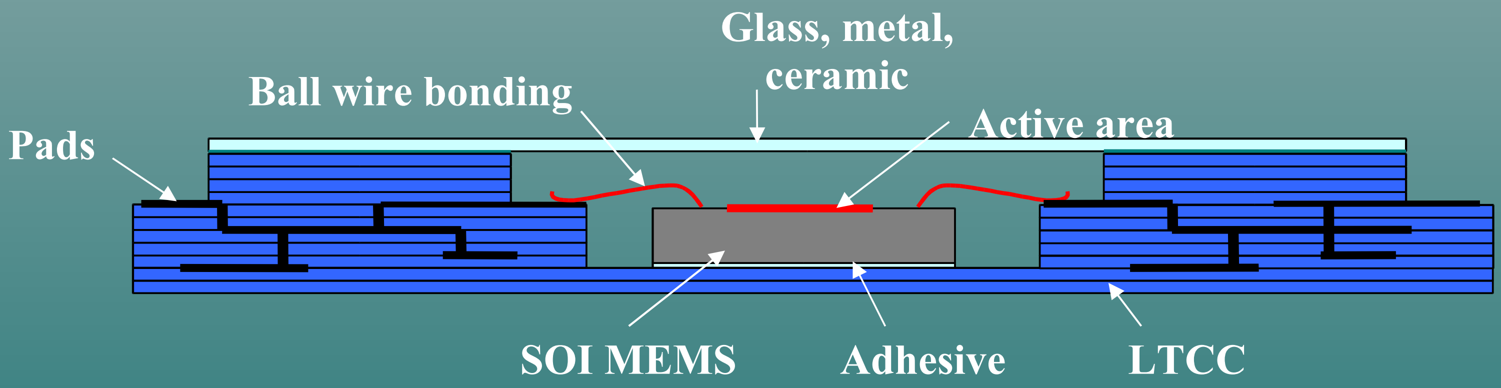
# Packaging dimensions

| | Top | Bottom |
|---|---|---|
| External pads [μm²] | 1000x10 | 640 |
| External pad´s pitch | 1000<br>00 | 1850<br>diam |

[μm]

Specific dimensions for Top and Bottom models

# Top Contact Model

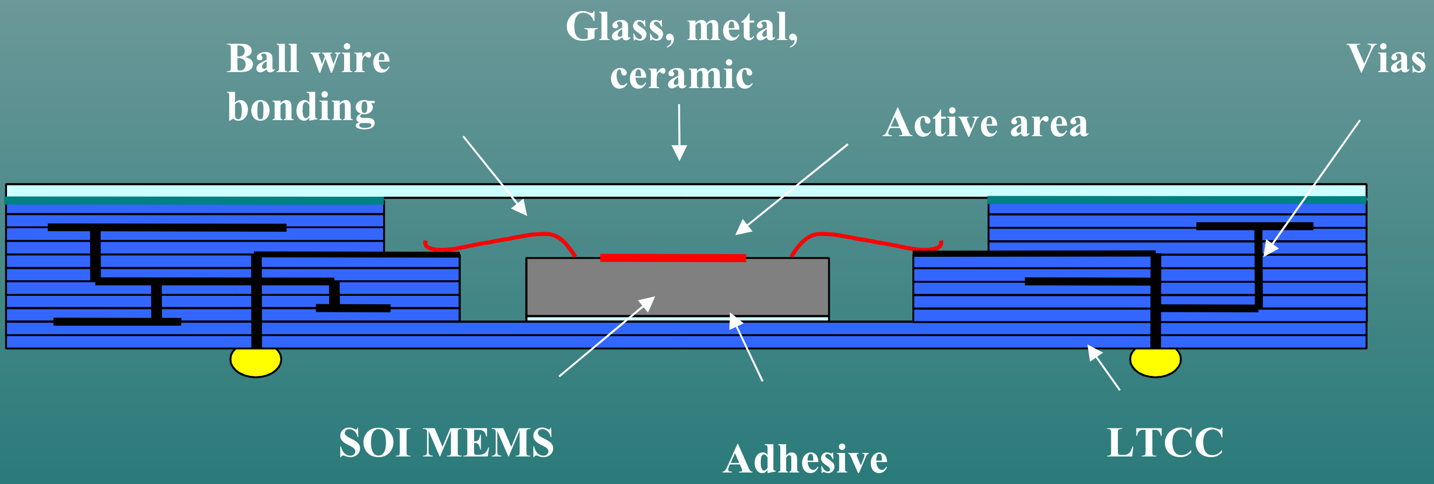


# Top Contact Model

Layers description:

- layer #1-2 die support
- layer #3-5 cavity for die
- layer #6 electrical connections
- layer #7 pattern for cavities
- layer #8-12 cavity for wire bonding

# Bottom Contact Model



# Bottom Contact Model

Layers description:

- layer #1-2 die support
- layer #3-5 cavity for die
- layer #6 electrical connections
- layer #7 pattern for cavities and vias
- layer #8-12 cavity for wire bonding

# Selection of Materials (I)

- DuPont 951 AT

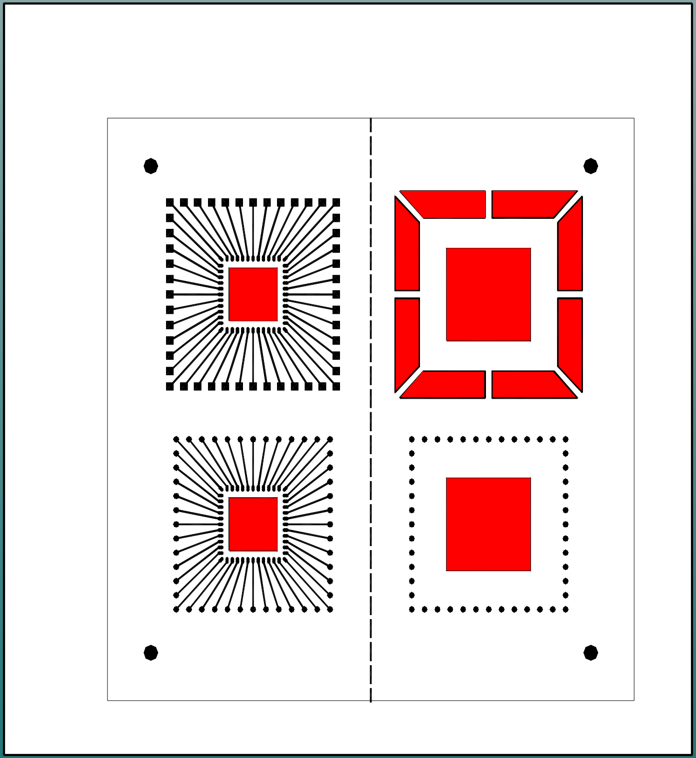
| Property | Performance |
|---|---|
| Fired thickness | 96.5 µm |
| Dielectric constant at 1 MHz | 7.8 |
| Shrinkage (x,y) | 12.7 % |
| Shrinkage (z) | 15 % |
| CTE | 5.8 ppm/°C |
| Young Modulus | 152 GPa |
| Thermal conductivity | 3.0 W/mK |

# Selection of Materials (II)

- DuPont 6148 Ag Cofire Inner Conductor
  - High conductivity metallization
  - Good inner layer compatibility

- DuPont 6141 Ag Cofire Via Fill
  - High density
  - High conductivity

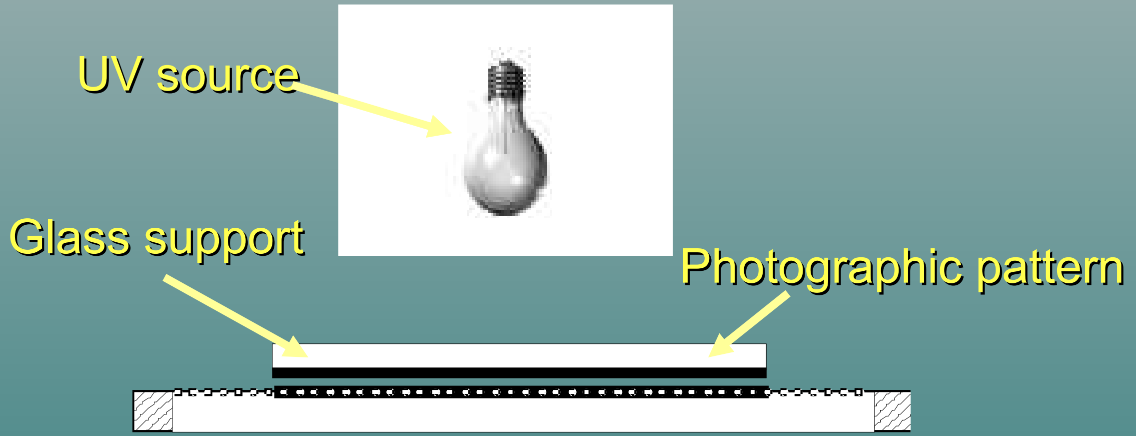
# Mask design

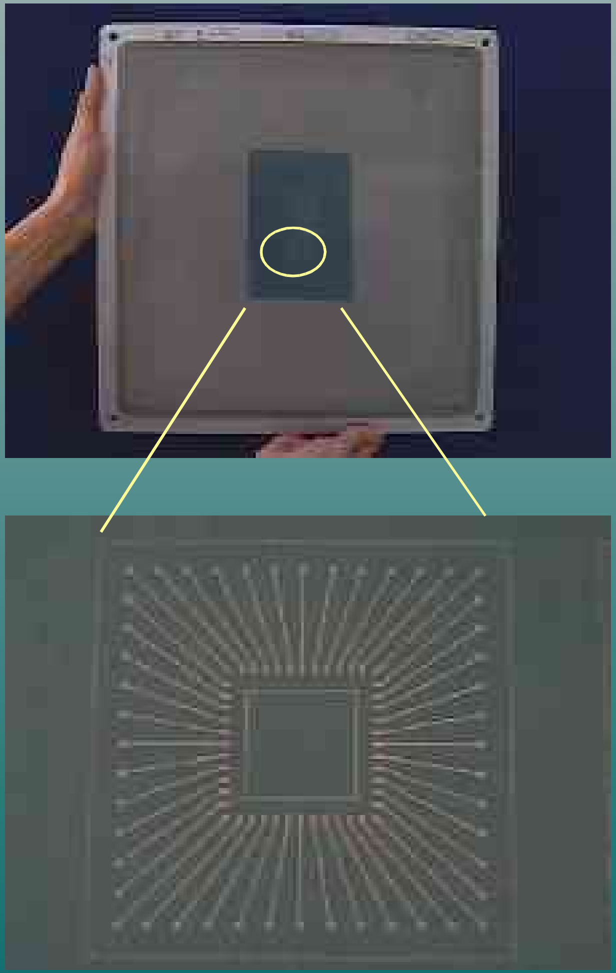


Top contact

Bottom contact

# Mask Fabrication

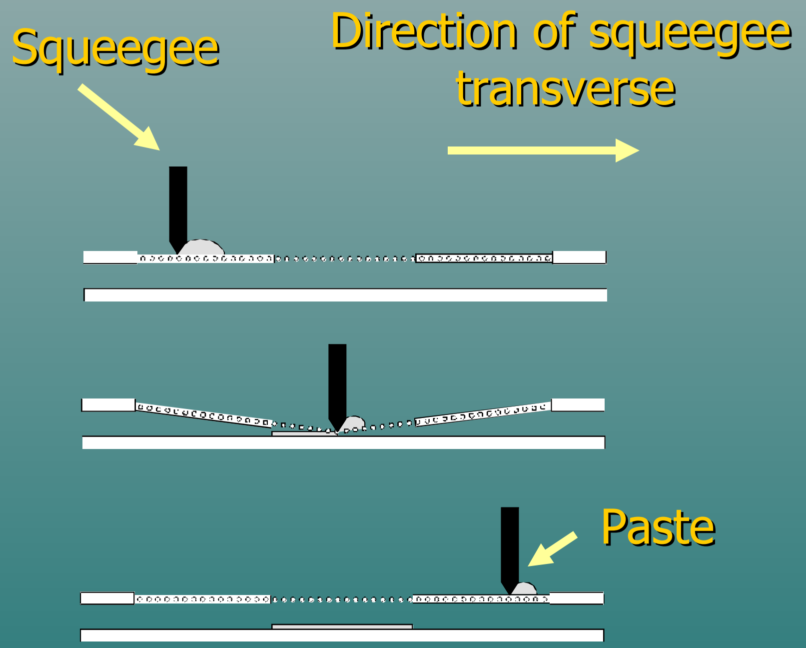




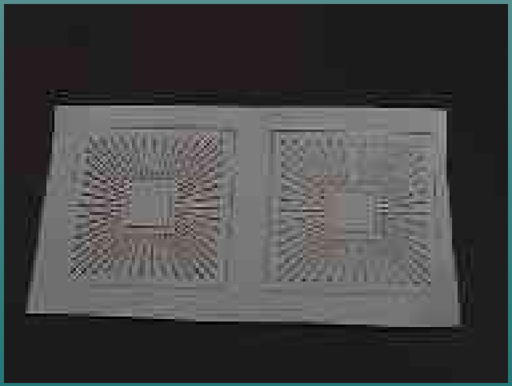
- Patterns transferred to the screen by photolithography
- Stainless steel mesh screen:

  300 mesh

# Screen Printing Process



- Screen printing of conductor lines with Ag thick film paste (DuPont 6148)
- Dried at 120°C during 30 min.

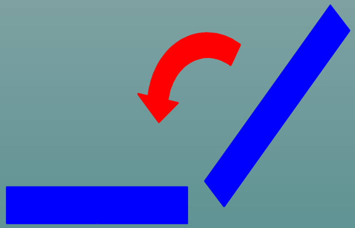


# Package Fabrication (I)

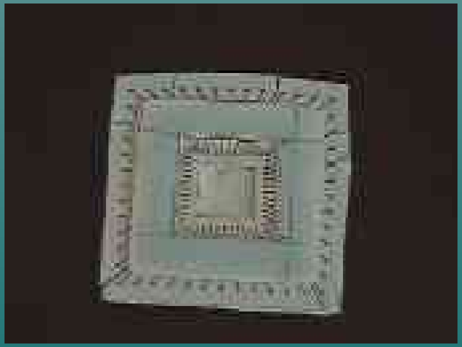
- Step 1: the sheets are cut and pre-conditioner at 125°C during 30 min.
- Step 2: lamination (1 kg.mm$^{-2}$ at 100°C during 3 min)
  - (A) Layers #6, #5, #4, #3 and #7, #8, #9, #10
  - (B) Layers #2, #1 and #11, #12
- Step 3: Forming cavities and punching of via holes of Ø=300μm by hypodermic needle
- Step 4: lamination of (A) + (B)

# Package Fabrication (II)

- Step 5: Cut and flipped of layers #7 to #12 over layers #1 to #6



- Step 6: Final lamination



Low lamination pressure

High lamination pressure

# Co-Firing Process

Co-fired at three plateaus:

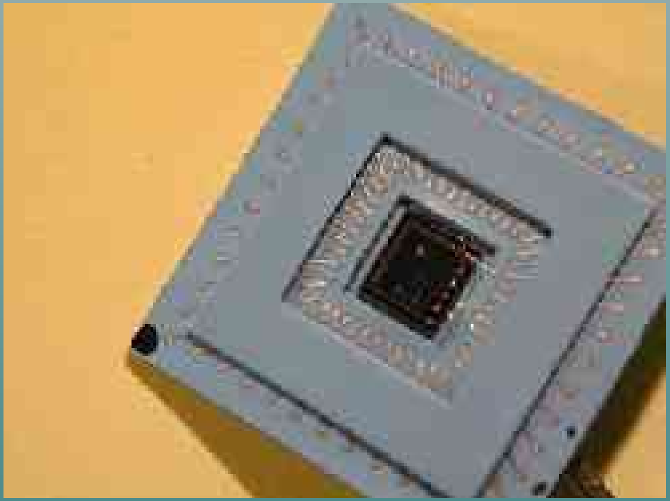
- 200°C burn off organic constituents
  slope 6°C.min$^{-1}$
- 500°C glass frit softening
  slope 4°C.min$^{-1}$

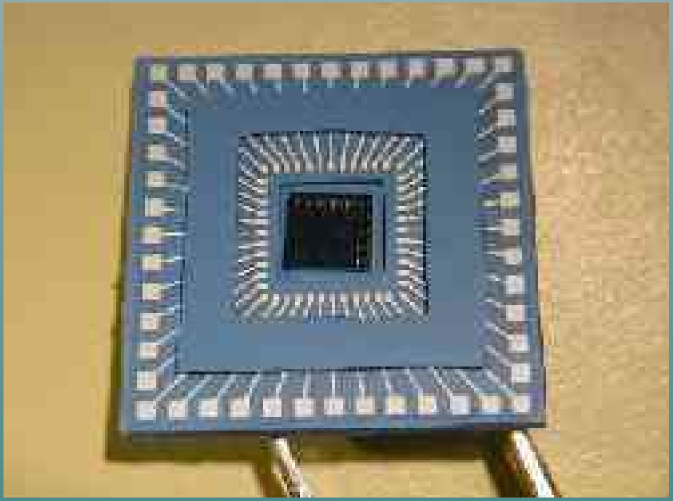
- 850°C sintering process
  slope 6°C.min$^{-1}$

# Assembly Prototypes

- Die attach adhesive: Dow Corning 7920
- Wire bonding - Au wire ∅ = 25 μm

# Top contact model

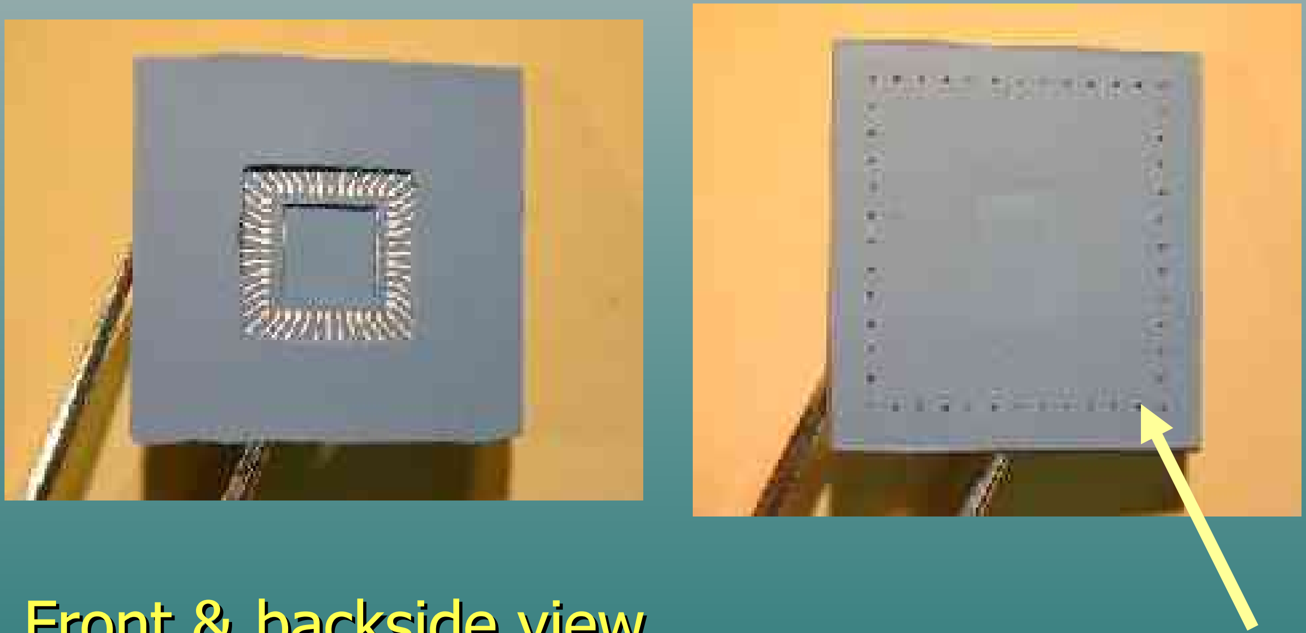




Die´s cavity height = 386 µm

Total height = 1160 µm

# Bottom contact model



Vias

Front & backside view

vias ~ 200 μm

# Case Study II: Passive RFID

- This typical chip is used in “passive” transponder application

- It does not require a battery power source

- Instead, RFID is powered by an electromagnetic energy field, transmitted by the reader

# Package Design

- First level packaging
  RFID Die on $AL_2O_3$

- Second level packaging
  Integration of antenna + 1st level pack.

Two models were proposed for the antenna:

- multi loop (ML), a 2D-structure flat square spiral coil

- uni loop (UL), a multi layer square loop in a 3D-structure

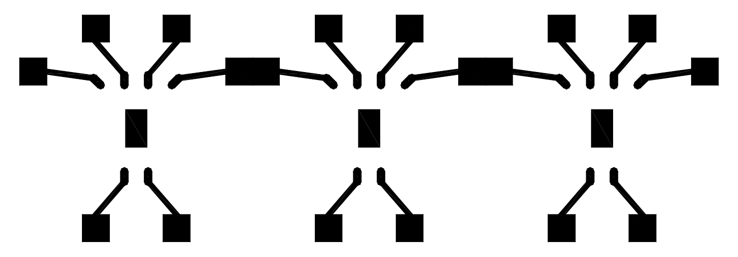
# Selection of Materials

- DuPont 951 AT LTCC
- DuPont 6148 Ag Cofire Inner Conductor
- DuPont 6141 Ag Cofire Via Fill
- EM-Microelectronic device -EM4006: 13,56 MHz read only

# Mask Design (I)

First level package

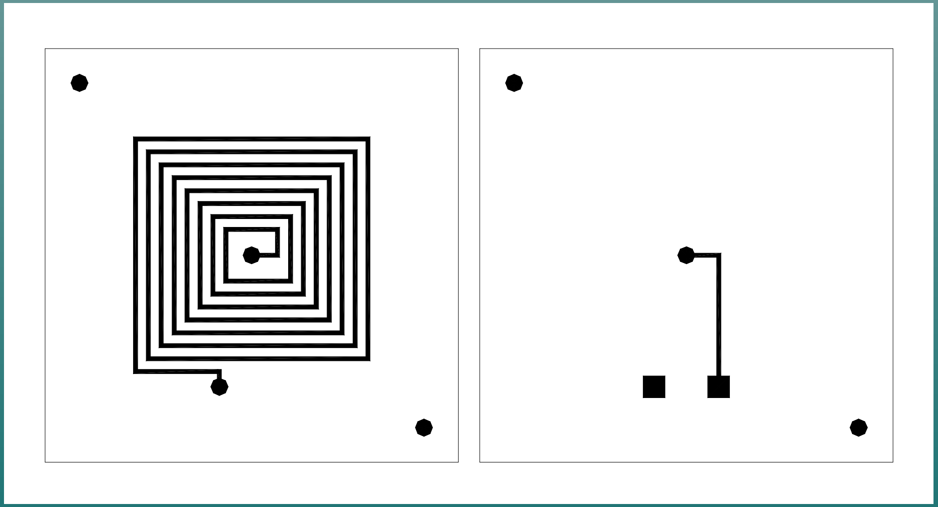
- # of pads: 6
- external pads: 1000 x 1000 µm
- internal pads: 300 x 660 µm
- internal pitch pads: 880 µm
- line width: 200 µm



# Mask Design (II)

Second level package: ML

- # of spiral: 8
- # of layers: 2
- line width: 200 μm



Layer #1 Layer #2

# Mask Design (III)

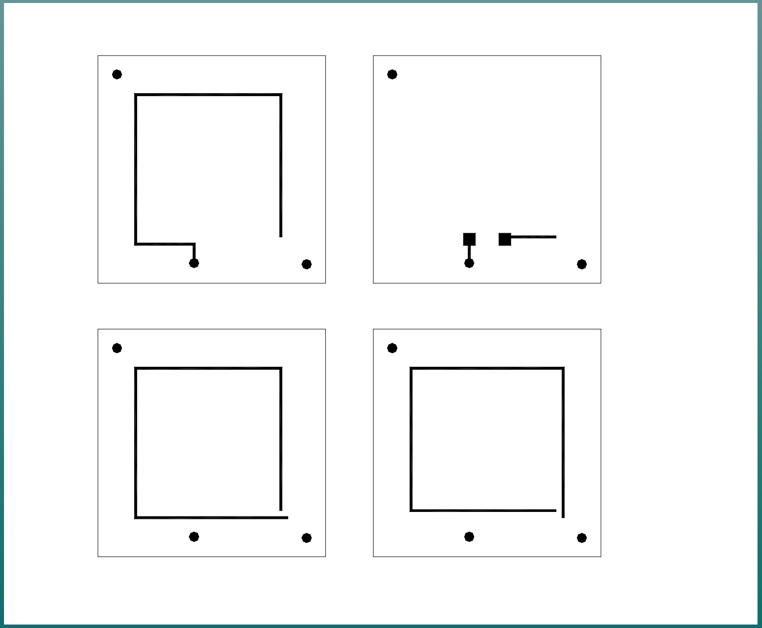
Second level package: UL

- # of spiral: 3 + 2 n (n = 0 -> i)
- # of layers: 4 + 2 n (n = 0 -> i)
- line width: 200 μm

Layer A: Top

Layer D: Bottom

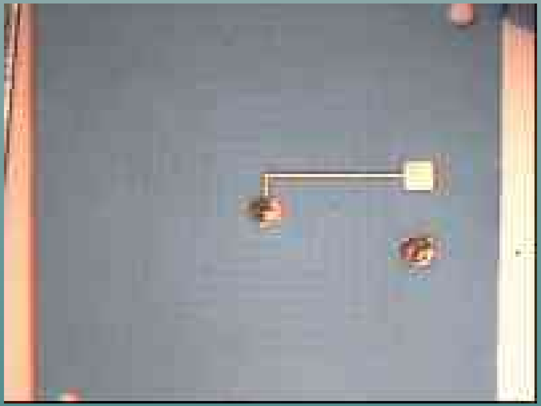
Layers B & C: internal



# Package Fabrication & Assembly Prototypes

- Screen Printing, Lamination & Co-firing Process
- Die attach adhesive: Dow Corning 7920
- Wire bonding - Au wire ∅ = 25 μm

# First Prototypes



ML antenna

UL antenna

1st level package

# Conclusions and Future Works

- Packages on & in LTCC were performed:Microactuator & RFID applications

- Good results in the fabrication of multilayers, cavities & vias were obtained

- Co-fire process was controlled (shrinkage, lamination)

- Future works: Electrical characterization of the prototypes

# Acknowledgments

- USP–Laboratório de Sistemas Integráveis [LSI]
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