Packaging for MEMS

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PASI on MEMS
6/21/04
MEMS Devices in Bewildering Variety have been demonstrated on the surfaces of wafers.

Cheng, Hsu, Lin, Nguyen, Najafi
U. Michigan, UC Berkeley

Kim, Lee, Lee, Sun, Seoul National

Xie, Fedder, CMU

Hsu, Clark, Nguyen, U Michigan

Klatidas, Linderman, Bright
U Colorado

All from Proceedings, MEMS’01
Interlaken, Switzerland (Jan, 2001)

None in Products
What are the barriers to MEMS Insertion?

cost and development time

MEMS is slower, more expensive, and harder to scale than VLSI

reliability

this is more art than science in MEMS

lack of standard processes, universal foundries

MEMS is a very big collection of diverse tools and materials

marginal or poor performance

drift in inertial sensors and resonators, selectivity in chem sensors
Is Packaging a barrier to MEMS Insertion?

cost and development time
   packaging adds a lot of cost and time to MEMS products.

reliability
   packages can improve reliability.

lack of standard processes, universal foundries
   all MEMS devices require custom packages – nothing is standard

marginal or poor performance
   better packaging can allow device optimization for performance.

This is not just a problem in the MEMS industry, by the way…
Microelectronics Packaging Today

Desktop Pentium 4 (top view)

Best modern technology in electronics layer

(side view)

Lian Zhang
Microelectronics Packaging Today

Desktop Pentium 4 (top view)

Best modern technology in electronics layer
Ancient “technology” in thermal layer

(side view)

Lian Zhang
The growing size of the thermal solution is a source of:

- Mechanical failure problems
- Weight problems
- System size for multi-processor systems (servers)
- Significant added cost
- Reliability problems (fan)
- Crowding away the power conditioning elements

Things are getting worse fast…
Cooligy develops thermal management components based on electro-osmotic pumps and novel microscale heat exchangers

The company was founded in September 2001 by Stanford Mechanical Engineering Faculty Goodson, Kenny, and Santiago

Cooligy has grown to 37 employees with $35 million in venture funding as of June ‘04
Cooligy’s goal is to introduce closed-loop liquid cooling into desktop and laptop computers.

Market Survey Question: Will your next computer include liquid cooling?
Example: Pentium P2 System: 45W processor operating at 1.4 GHz.

Total volume of 3”x 3”x 2” Total Cost > $5.

This is a good example of 1999 cooling system design

Extruded Aluminum heatsink with fan.

All hardware mounted directly on back of die/spreader.

Thermal conduction forces fin design that blocks all space under heatsink.
Example: Gateway SFF Desktop 70W processor operating at 2 GHz.

Total volume of 4”x 4”x 3”+ block  Total Cost > $15.

This is an example of a P3 Processor from early ‘02

Heat Pipes used to move heat a few cm from processor to use airflow through vent for cooling.
Liquid Cooling is already in your computers.

This example is typical of P4 desktop computers since mid 2002.

This approach still forces the box designer to bring the air to the microprocessor.

Example: Dell Precision 3500: 90W processor operating at 3 GHz.

Total volume of 4”x 4”x 6” Total Cost > $20.
Example: Apple Mac G5: Dual 90W processors operating at 2 GHz.

Total volume of 7”x 7”x 7” Total Cost > $50.

This unit uses heatpipes to distribute heat from a pair of processors throughout a very large fin array.

The entire computer chassis is designed to provide low-noise airflow and heat distribution.

This is an example from late 2003.
Market Survey Question: Will your next computer include liquid cooling?

In fact, most desktops and all laptops have had liquid cooling (heat pipes) for a few years already.

Pumped, liquid cooling is also already appearing:
- Toshiba began shipping a water-cooled laptop in ‘03
- Apple announced a water-cooled G5 Desktop to be shipped in late ‘04
A Challenge for Microprocessor Packaging

This problem is expected to worsen quickly.

Hotspots cause additional problems that cannot be solved by Cu heat spreaders.

Power Q (W)

ITRS

Si chip

Hotspot (e.g., floating point)
HERETIC Program (‘99-’02)
funded >8 projects exploring methods for cooling and thermal management

VISA Program (’02-’04)
funded projects exploring vertical integration of sensors/electronics

MARCO Interconnect Focus Center (’99-??)
large consortium looking for methods for high-density interconnects, mixed signals, thermal management, 3-D electronics.

DARPA 3D IC BAA Open (’04-’09)
Proposals being solicited for technologies that enable 3-D stacked architectures.

HERMIT Program (’03-’08)
MEMS devices and packaging for harsh environments

Packaging/integration is showing up in DARPA
Encapsulated MEMS

Thomas Kenny, Rob Candler, WooTae Park, Holden Li, Matt Hopcroft, Renata Melamud, Bongsang Kim, Sarubh Chandorkar
Stanford University

Markus Lutz, Aaron Partridge, Gary Yama
Bosch RTC

Amy Duwel, Mat Varghese, Draper Labs

Supported by Bosch and CIS Seed, Transitioning to DARPA HERMIT Program Support
Another option is to develop a wafer-scale post-process bonded package.

This approach is widely used in industry, but suffers from significant disadvantages.

- Lost Die space
- Yield
- Temperature budget
- Cost

Device <20% of Die, Bond Ring is 60% of Die

Example numbers Adapted from Bosch Accelerometer
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One option is to develop a post-process, locally-bonded, thin-lid technology.

Liwei Lin and others at Berkeley are working on localized bonding methods to reduce lost die area and post-process thermal budget. Advantages include low temperature, post-device processing. Disadvantages include need for electrical interconnect during packaging process, lost die space, and questions about yield.


L. Lin, “MEMS Post-Packaging at the Wafer Level”, Invited Presentation, InterPACK 2001
In most MEMS processes:

Design and Process are optimized to improve device performance.

Die Separation is a traumatic event.

Custom processes for packaging are developed after the MEMS devices have shown interesting performance.

“90% of the cost of a MEMS device is in the package”
Packaging is a Problem for MEMS

Recommendation

Think about the final package/test environment when designing the MEMS part. Some things that are trivial in design can significantly impact package cost or test cost.

Incorporate Formal Design Methodologies: Design for Manufacturing, Taguchi, QFD,... Rarely used in academic MEMS or “Start-up MEMS”, but an essential component of a real MEMS product

Be realistic about package costs, test costs, etc in the cost model for your technology. Use formal methods for tracking cost during development.
We propose:

Turn a “problem” into an opportunity
We propose:

Integrate packaging into the MEMS fabrication process.

Develop and optimize designs to overcome package process compromises.

Leverage opportunities that come from a package-integrated process for performance improvements.

Avoid all back-end custom handling and packaging. Move back towards conventional chip packaging approaches.

Deliver unique MEMS capabilities without the usual baggage, and with some new features.
Start with a “generic” MEMS device made from silicon, prior to being released from the substrate by HF. Silicon layer may be single crystal (SOI), or poly-si (Bosch epi-poly structural material, for example).
Deposit a thick (3-5 µm) non-conformal Low-Temperature oxide. This oxide fills and seals structures around the device, producing a complete sacrificial encapsulation.
Deposit Thick Epi-Poly. This forms poly where grown over LTO, and forms single-crystal Si where grown over single-crystal Si.

Deposition rates of up to 3 µm/min achieved in conventional Epi-Si reactor at Stanford, and in a production environment at Bosch.
The encapsulation oxide is removed in a Vapor HF etcher, developed by Bosch (Prototype installed at Stanford), and the device is sealed by a second non-conformal LTO. TEOS and other thick oxide processes being explored.
An opening in the oxide over the interconnect allows formation of a bond pad.
The interconnect structure is isolated from the surrounding Epi-Si layer by an annular oxide seal, and makes electrical contact to a doped layer on the device level of the structure. Interconnects of this architecture can be fabricated with 5:1 aspect ratio, and may be as small as 20 µm in diameter.
Wafer-Scale Package

Package can withstand high pressures
- 25 µm cap can withstand 100 ATM for Injection Mold Packaging

Very Little Lost Die Space
- Only 10-20 µm needed for “bond ring”
- Surface over device may be used for wire-routing.
- Entire process can be pre-CMOS
Wafer-Scale Package Status

suspended resonator beams

Si  oxide  epitaxial Si
This is a fully-operational device with interconnects, release, encapsulation, and hermetic seal.
Wafer-Scale Package Recent Status

These are some of the least-interesting MEMS devices you’ll ever see. All the interesting details are hidden from view by the encapsulation.

These details are also protected from dicing, handling, dust,…

These parts were dump-rinsed, diced, hosed, scrubbed, and glued without any special handling.
Features: High Yield (for academia)

We were able to achieve yield of 96% during a recent fabrication run, with all steps at Stanford CIS (except for CMP at BSAC).

Film Encapsulated devices, Each device is 0.8mm²
Sealed and Vented cavities formed in same process on same wafer, through adjustment of vent sizes
We have shown encapsulation survival to 100 ATM and to 250C for a 200µm seal area.

Example Accelerometer Designs

Piezoresistive


Capacitive

“differential-capacitive accelerometer”
Robert Bosch Corporation
Wafer-Scale Package Recent Status

View from underside - Herring-bone pattern of release vents through polysilicon encapsulation provides highly-uniform access for HF Vapor. These vents can be re-sealed by 5 µm CVD oxide growth as a last step.
Features: Reduce die size for inertial sensors

Substantial reductions in die size possible through elimination of bond rings and other package elements.

Optimization with respect to thermal noise, piezoresistor performance necessary for further scaling.
Reduce die size

Already able to reduce die size 70% compared to wafer-wafer bonding. Same Functionality!

Photos by Silvia Kronmueller, Bosch

Micro Structures & Sensors Lab
Working Accelerometers

Functional Parts of many types within encapsulation.
CMOS Integration on EpiPoly Cap Layer
There is growing interest in Silicon Resonators as filters and oscillators for Telecommunications

Opportunity:
• Potential for integration with IC for “Single-Chip systems
• High Q, tunable frequency, good range, nice properties
• Low Cost

Barriers:
• MEMS resonators need to be packaged
• Silicon has a high temperature coefficient of modulus - frequency drift more than 10x worse than quartz resonators
• Co-Fabrication with CMOS not demonstrated.
• Lifetime, Reliability not understood.

Excellent demonstration platform -> Show that MEMS is Mature Technology for Packaging of Integrated Systems
Encapsulated MEMS Primary Goals

Ultra-Stable High-Q, 100 MHz Resonators and Encapsulated High-Performance Inertial Sensors

• Leverage established encapsulation process to build test devices from day one. High yield, stable operation, rapid design-to-parts capability is already available.

• Study and model relationships between Q, Designs, Frequency, Aging, Clamping, Materials, to support development of high Q at 100 MHz.

• Attack Temperature Coefficient of Frequency (TCF) through combination of capacitive compensation, TCE compensation, and direct thermal regulation. We need an improvement of more than 1000x in TCF
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To measure the pressure within the encapsulation, we need an encapsulated pressure sensor.

Fortunately, it is possible to design resonators that will be sensitive to pressure because of damping

Elsewhere in this project, we’ll be optimizing for immunity to pressure variations.

For this task and milestone, we have custom resonators that are dominated by the pressure damping effect in the range of interest.
Center-anchored, double-double design.
Frequency ~150 kHz, Q~33,000
Pressure and Leak within Encapsulation

HERMIT Part A Calibration.

Q~30,000 corresponds to pressure at or below 0.01 Torr
Long-Term, Continuous Test

NETWORK ANALYZER
HP4395A

MULTIPLEXER
Agilent 3499B

MULTIMETER
FLUKE 8840A

DC BIAS
Agilent E3632A

TEMP. CHAMBER
TESTEQUITY1000

STIMULUS

RESPONSE

RESPONSE

OTHER SIGNAL

TEMP. SIGNAL

BIAS
Long-Term, Continuous Test

Permanent Installation for continuous monitoring of a set of resonators
Goal - Gather Solid Data for Phase 1 Milestone.
Prepared to gather 1 year of continuous data from 12/03 parts.
Q-Stability -> Pressure Stability inside Encapsulation
Path to “ultra” Stability

Thermal Control within the Encapsulation
- Develop designs and methods for direct temperature regulation within the device encapsulation
- “Single Oven” and “Double Oven” approaches possible.
- Begin with heated resonators, and move towards ovens.

Diagram:
- Oxide
- Heater
- Thermometer
- Contacts
- epi-polySi
- Crystal Si
- Substrate
- Drive Electrode
- Resonator
- Sense Electrode
Heated Resonator Designs

Thermal Control within the Encapsulation
- Preliminary Lumped Parameter Models for Heated Resonator Design. This is a precursor to Design of Heated Encapsulation

STANFORD Micro Structures & Sensors Lab

BOSCH
Encapsulated MEMS

Summary

• Silicon Resonators do not currently offer acceptable performance for many applications. Stability and packaging cost are barriers.
• A wafer-scale, MEMS-based encapsulation process for resonators has been developed through a Bosch/Stanford collaboration with support from Bosch, DARPA and CIS.
• This encapsulation is a platform for development of performance improvements, enhanced reliability, and cost reduction for silicon resonators. Integrated compensation and regulation is possible to improve TCF.
• This is an example of an ideal CIS-fostered collaboration that is producing good things for all participants ($$, IP, PhDs,...)
Long-Term Goal: Show that MEMS is a Packaging Technology which offers:

- Standardization
- Improved yield
- Reduced cost
- Reduced Time to Market
- Improved Reliability
- Performance Enhancements
- Integration with CMOS,…
Questions???