Microfabrication Process for a Silicon Thermal Gas Sensor

Taller de "Tecnologías MEMS para Sensores"
29-31 de julio de 2002, Buenos Aires

RED IX.I: TESEO
"Tecnologías para el Desarrollo de Sensores y Microsistemas"

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Summary

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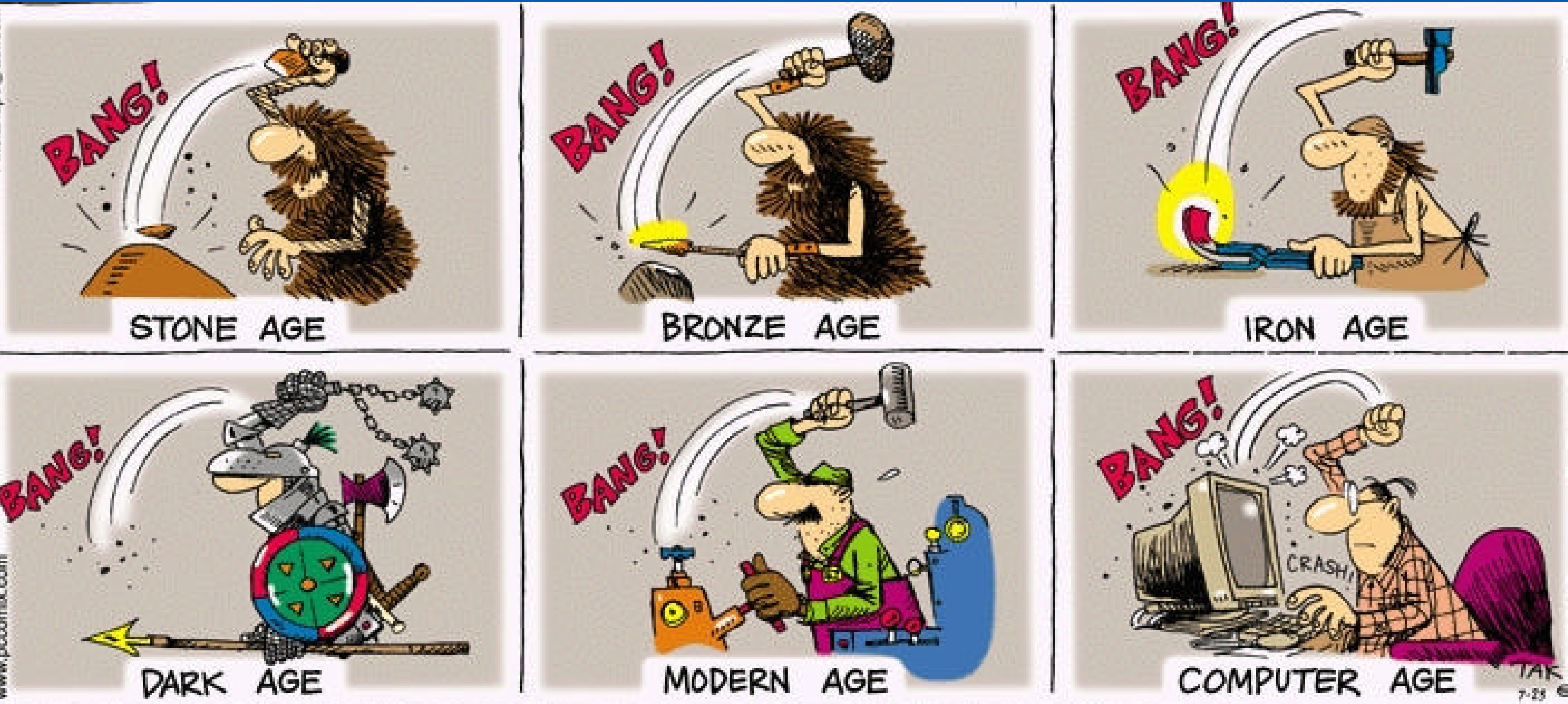
- Device Characterization
- Gas Measurements

Technology Evolution



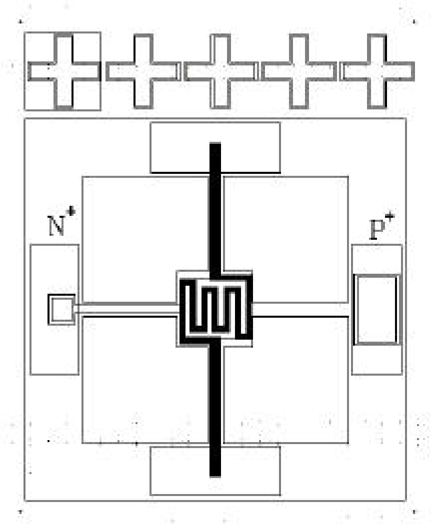
Introduction

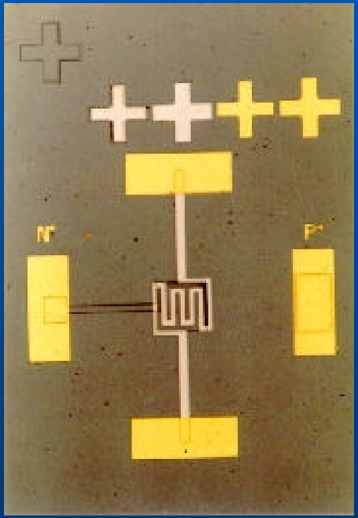
- **Doctoral Thesis in Physics**
  - **Universidade Federal do Rio Grande do Sul**
  - **Advisors in Brazil :**
    - **Prof. Dr. Wido H. Schreiner**
    - **Prof. Dr. Sérgio Ribeiro Teixeira**
- **Experimental Work**
  - **Microfabrication Laboratory - Electrical Engineering Dept.**
  - **University of Pennsylvania**
  - **Advisors in US**
    - **Prof. PhD. Jay N. Zemel**
    - **Prof. PhD. Jorge J. Santiago-Avilés**
  - **Laboratory Advisor and Motivation “Make no mistakes or die”**
    - **Vladimir Dominko (Lab. Manager)**

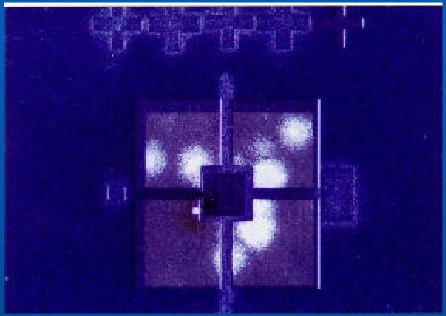
Project of the Device

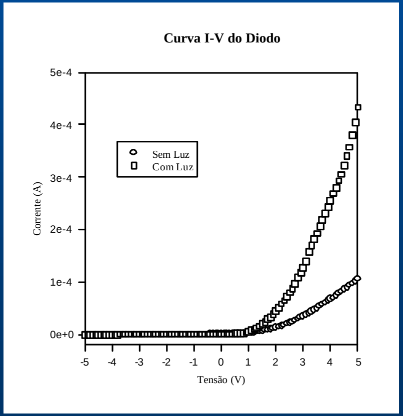
- **Initial idea:**
  - **Develop a device able to detect the reaction of H_2 / O_2 catalyzed by Pd at low temperatures. (£ 130 ^{o}C)**
  - **Use a diode as the thermometer instead of resistors, thermopiles or pyroelectric.**
- **Experimental Constraints**
  - **Small active area**
  - **Small thermal mass**
  - **Fast response**
  - **Simple (without any built-in electronics for signal conditioning)**
- **Pre-conclusions**
  - **Device must be based on a Silicon Membrane**
  - **It must have an integrated diode**

First Generation



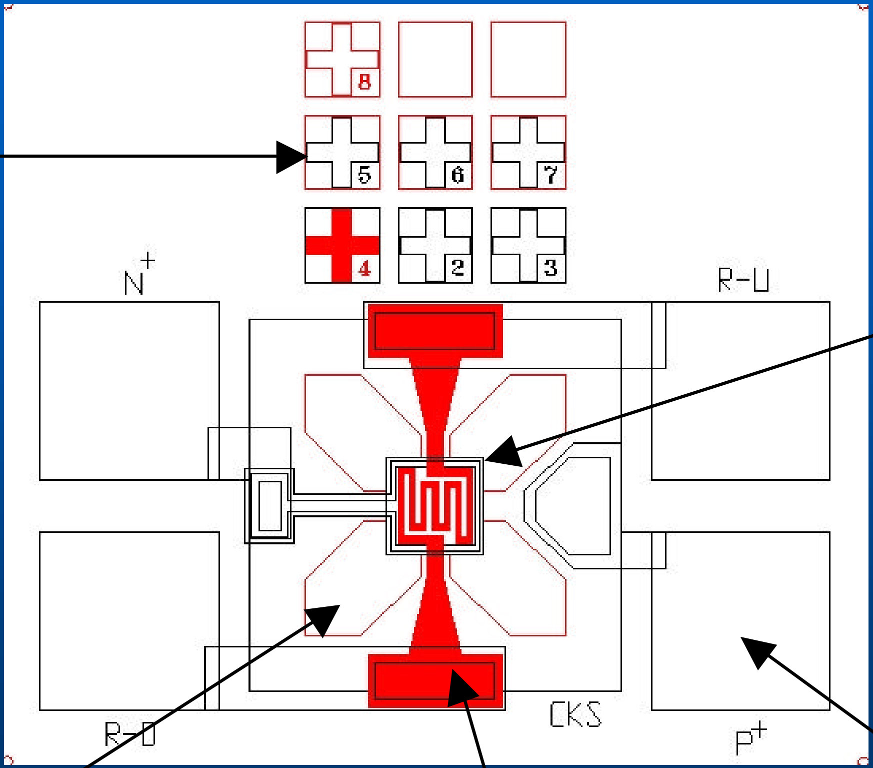






Second Generation

- **Problems in First Generation**
  - **High value of the diode series resistor**
  - **Depleted n^+ region**
  - **Mechanical fragility**
  - **Difficult external connection (silver epoxy)**
- **Solutions**
  - **p^+ doping of the whole surface (except n^+ region)**
  - **Increase width of the bridges and reduce length**
  - **Increase gold pad size**



Alignment marks

Active area

Gold pad

Diaphragm opening

Pd Resistor

Lithographic Masks

- Drawings
  - Cadkey (Autocad) - one device
    - Actual option (LASI Cad http://members.aol.com/lasicad2/index.htm)
  - Exported DXF
  - Pattern generator program
    - Creates a matrix of devices
    - Generates de codes for pattern generator
- Masks recorded on Emulsion Glass Plates (7 masks)
- Standard photographic development procedure

Print mask → Develop → Dry → Visual inspection → Store

Silicon Wafer Cleaning

- **Standard RCA Cleaning Procedure**
  - **Preliminary Cleaning:**
    - **Remove excess of fotoresist (when present)**
      - **Plasma O_2**
      - **Organic solvent**
    - **Boil wafers H_2O_2:H_2SO_4 (1:2) - 120 °C / 10 min (PIRAÑA)**
    - **Rinse in DI water (overflow) - 5 min**
  - **Remove organic contaminants and certain metals**
    - **H_2O-H_2O_2-NH_4OH (5:1:1)**
      - **H_2O_2 (30% unstabilized electronic grade)**
      - **NH_4OH (29% electronic grade)**
    - **Submerge holder in cold solution**
    - **Heat solution to 80oC - keep at this temperature 10 min**
    - **Rinse in DI water (overflow) - 5 min**

- Stripping of thin hydrous oxide film
  - Submerge wafers (without drying)
  - $HF:H_2O$ (1:50)
    - HF (49% electronic grade)
  - Room temperature / 15 sec.
  - Silicon surface becomes hydrophobic
  - transfer wafer to next solution immediately
- Desorption of remaining atomic and ionic contaminants
  - $H_2O:H_2O_2:HCl$ (6:1:1)
    - H_2O_2 (30% unstabilized electronic grade)
    - HCl (37% electronic grade)
  - Heat solution at 75-80^{o}C
  - Submerge wafers and keep for 10-15 min
  - Rinse in DI water (overflow) - 10 min

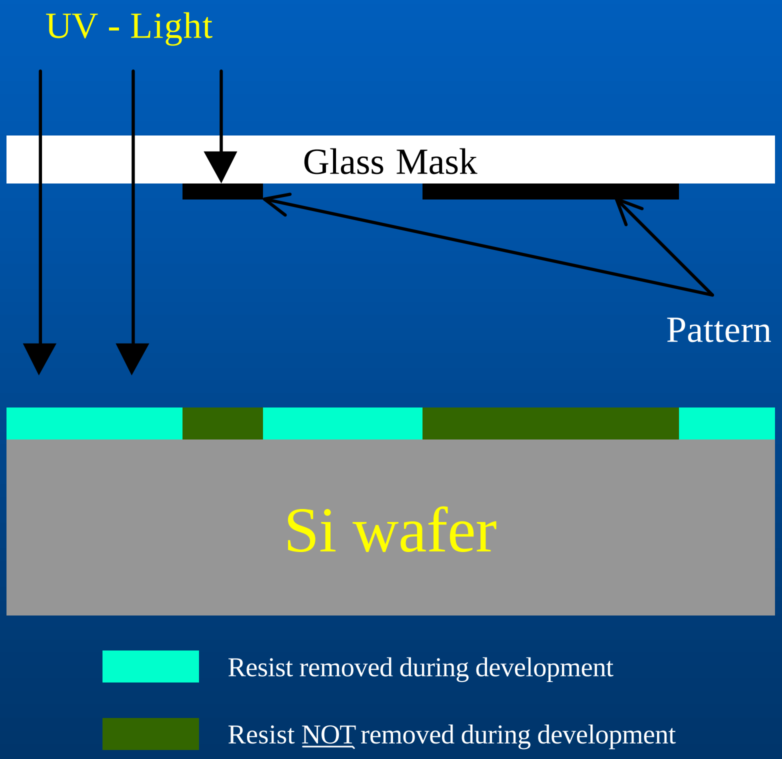
Process time ~ 1 hr

Lithographic Process

- **Positive Resist Process**

  Shipley S1400-27

  - **Wafer drying**
    - **Hot plate 120ºC / 10 min**
    - **HDMS - (5 min) Hexametildisilizane**
  - **Spin Coat 5000 RPM ® 1,2 µm**
  - **Soft-bake 90-100ºC / 10 min**
  - **Exposition 70 mJ/cm^2 (necessary)**
  - **Development**
  - **Extra exposition UV**
  - **Post-bake 100-120ºC / 4 min**



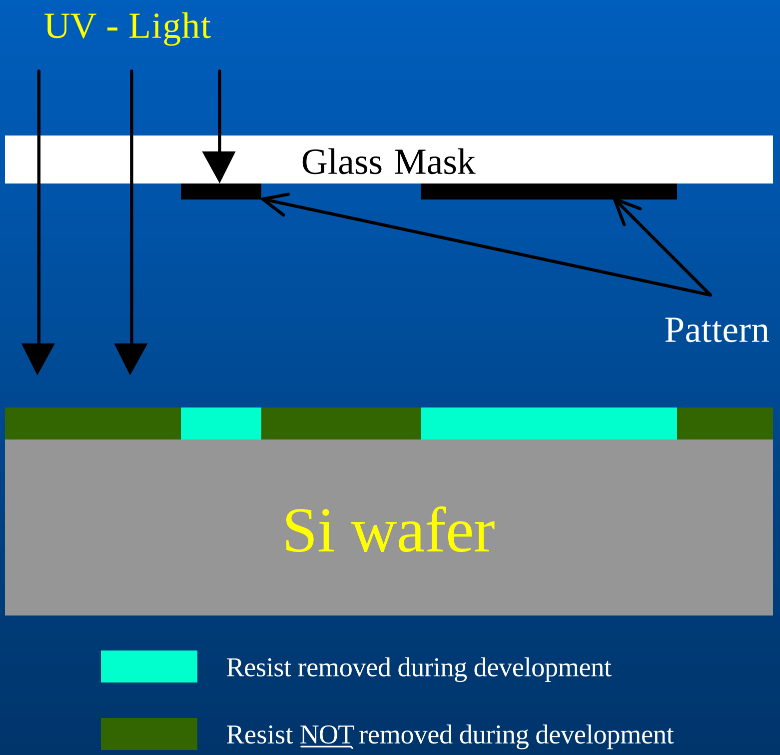
🟦 Resist removed during development

🟩 Resist NOT removed during development

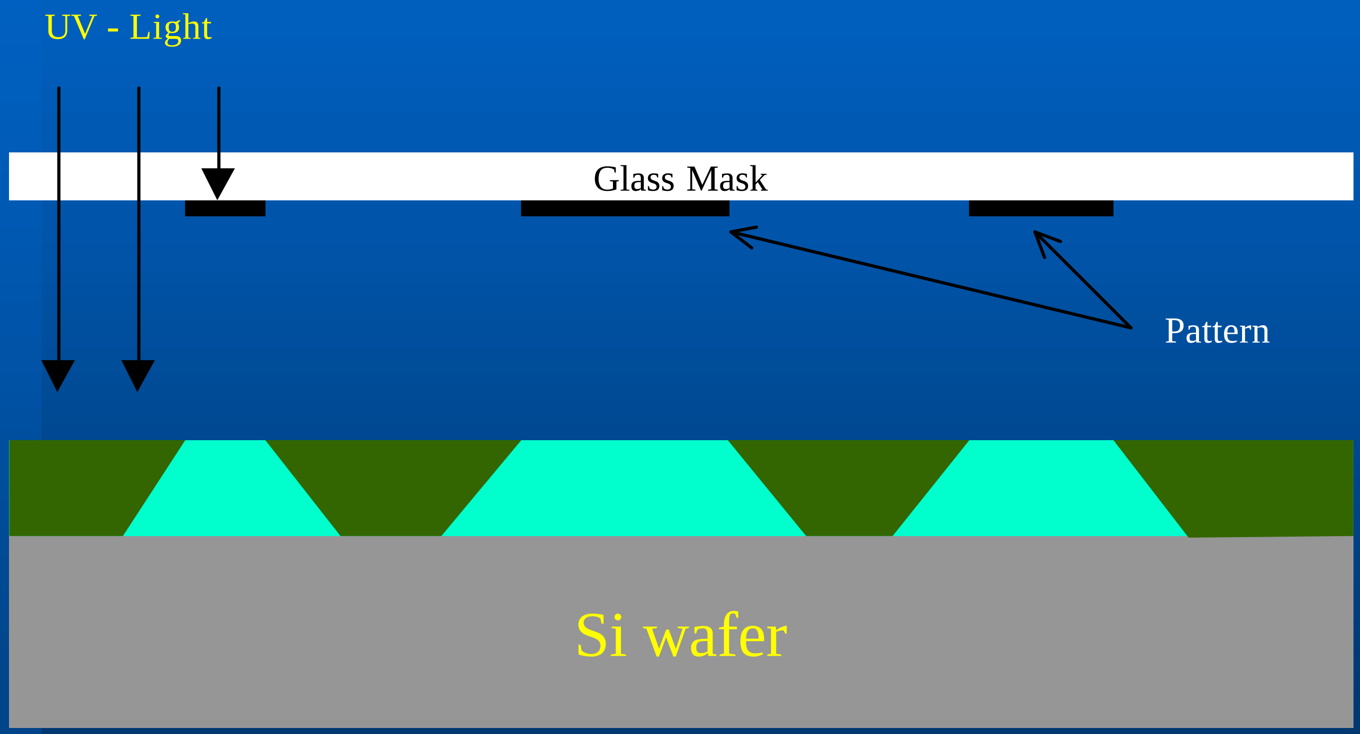
- **Negative Resist Process**

  Futurrex NR8-1000

  - **Wafer drying**
    - **Hot plate 120^{o}C / 10 min**
  - **Spin Coat 2000 RPM ® 1,3 µm**
  - **Soft-bake 130^{o}C / 60 sec**
  - **Exposition 90 mJ/cm^{2} (used)**
  - **Development**



Liftoff Negative resist profile



🟦 Resist removed during development

🟩 Resist <u>NOT</u> removed during development

Under-etch occurs during the development processing

Wet Anisotropic Etch

- **Application**
  - **3D structuring of silicon, channels, membranes, holes**
- **Procedure**
  - **Select etchant KOH, EDP (Ethilene Diamine Pyrochatecol), TMAH**
  - **Select concentration / Temperature**
  - **Example:**
    - **KOH 10% / 50 ^{o}C**
    - **13 µm/h Si[100] - 9 nm/h SiO_2**

Wet Oxidation

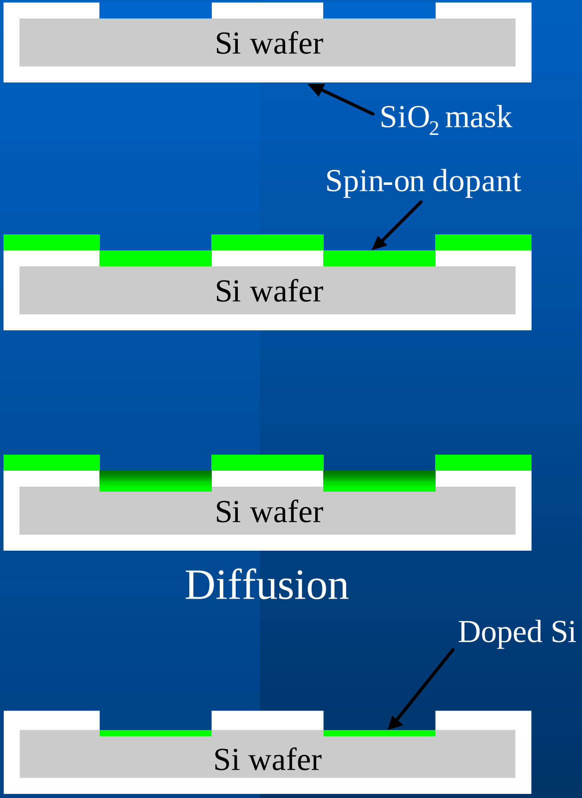
- Application
  - Mask / Low quality insulation
- Procedure
  - Heat up the furnace (appropriate temperature)
  - Wafers cleaned, etched with BHF, dryed
  - Switch from dry N_2 ® dry O_2
  - Dry O_2 flow ® load the wafers (slow)
  - Switch to $O_2 + H_2O_{vapor}$ (appropriate amount of time)
    - Si [100] - 1100^{o}C / 2 h ® ~ 0.7 µm oxide
  - Switch to dry O_2 (3 min)
  - Switch do dry N_2 ® (leave 3 min) unload the wafers (slow)

Dry Oxidation

- Application
  - High quality gate insulation (very thin)
- Procedure
  - Heat up the furnace (appropriate temperature)
  - Wafers cleaned, etched with BHF, dryed
  - Switch from dry N_2 ® dry O_2
  - Dry O_2 flow ® load the wafers (slow)
  - Switch to O_2 + TCE_{vapor} (trichloroethane) (appropriate amount of time)
    - Si [100] - 1100^{o}C / 2 h ® ~ 0.2 µm oxide
  - Switch to pure dry O_2 (3 min)
  - Switch do dry N_2 ® (leave 3 min) unload the wafers (slow)

Spin-on Doping

- **Advantages**
  - **Low toxicity ($POCl_3$, Bromines , ... ® ☠)**
  - **Easy to handle**
  - **Used dopants**
    - **P (Phosphorous) ® type n^+**
    - **B (Boron) ® type p^+**



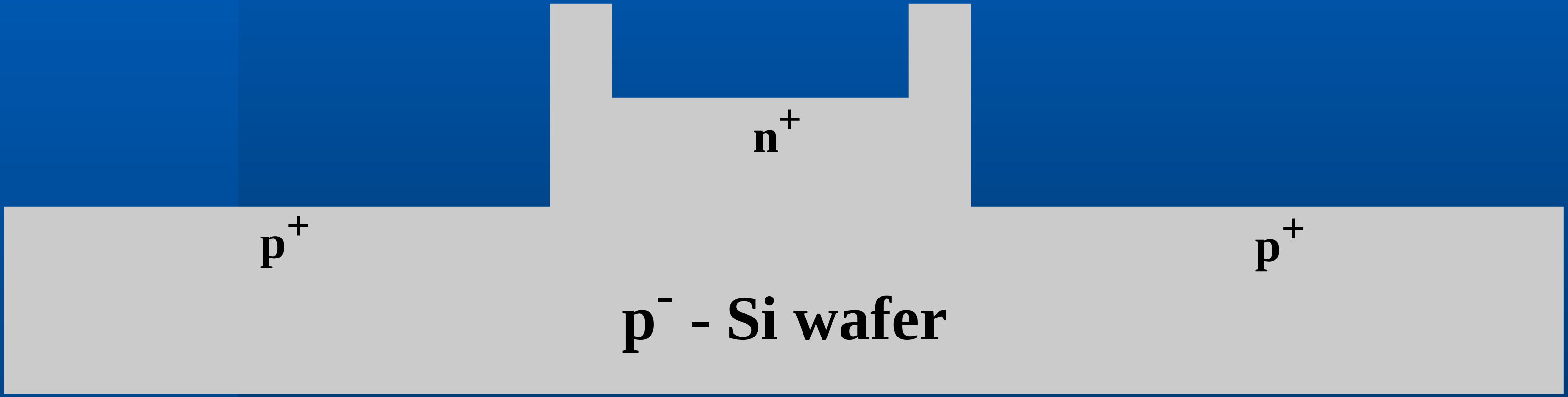
Diffusion

Dopant removal

Drive in

Mask oxide removal

Example of profile obtained to fabricate a p-n junction



Metalization Process

- Application ® contacts, wiring, vias, ...
- Deposition methods:
  - Physical
    - e-gun
    - sputtering
    - thick film (silk-screen)
  - Chemical
    - CVD (Chemical Vapor Deposition)
    - Electrochemical
- Patterning
  - Chemical etch
  - Liftoff technique

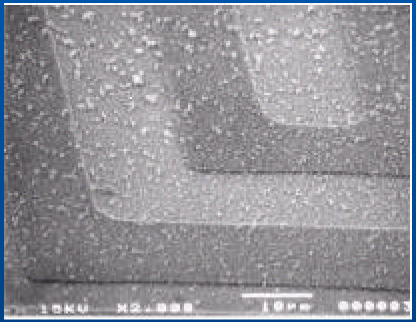
Chemical x Liftoff

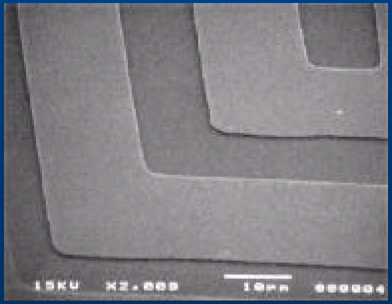

Open window

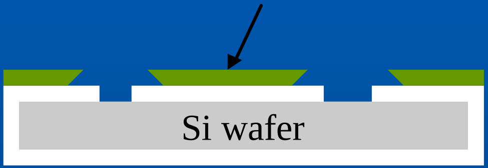

Metal layer


Patterned resist


Metal pad after etch and resist removal






Patterned Resist


Metal layer


Metal pad after resist removal

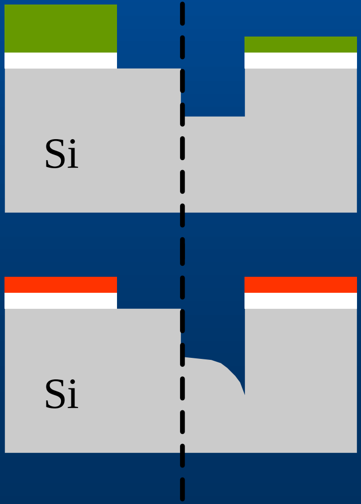
Plasma Etching (RIE)

- **Application**
  - **Window opening, channels**
- **Operation principle**
  - **Low pressure Plasma discharge**
    - **Gases: SF_6, C_2F_6, O_2, Cl_2,...**
  - **Original gases are broken into ionized reactive species**
- **Masking (for SF_6 plasma protection)**
  - **Resist**
    - **Advantages: no charge built up**
    - **Disadvantage: high etch rate**
  - **Metal**
    - **Advantages: low etch rate**
    - **Disadvantage: charge built up**

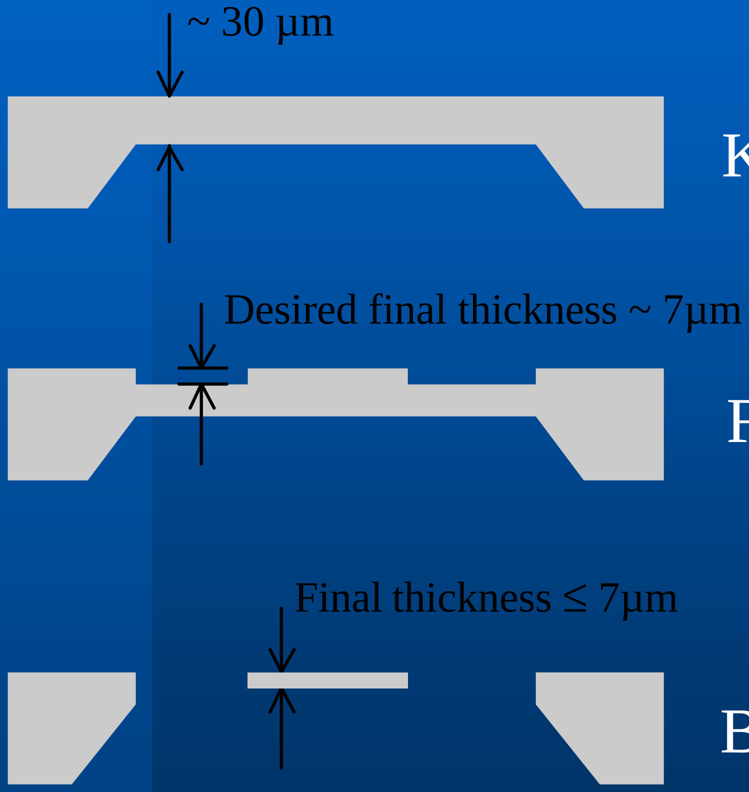
SF_6

Si → ~ 1,4 µm/min

Resist → 0,2 to 0,4 µm/min



Membrane Thickness Definition

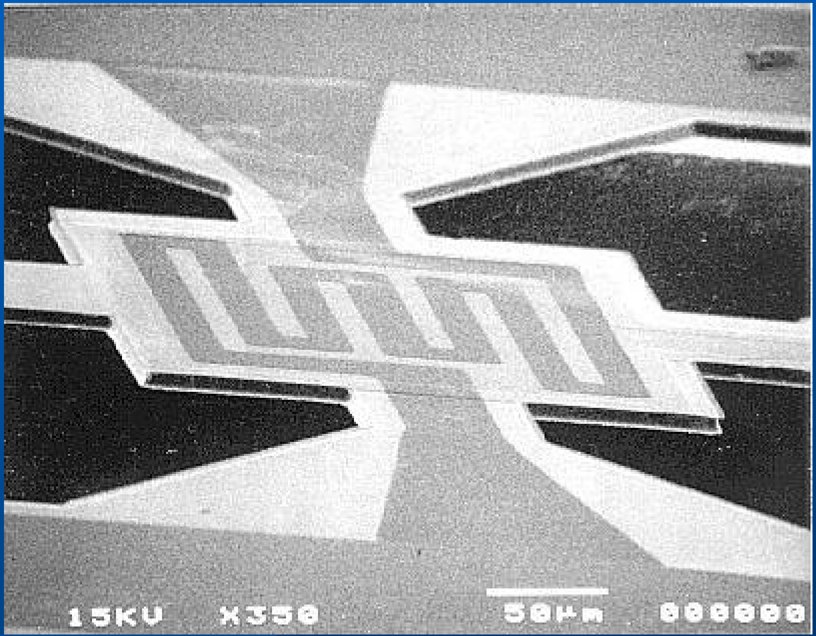


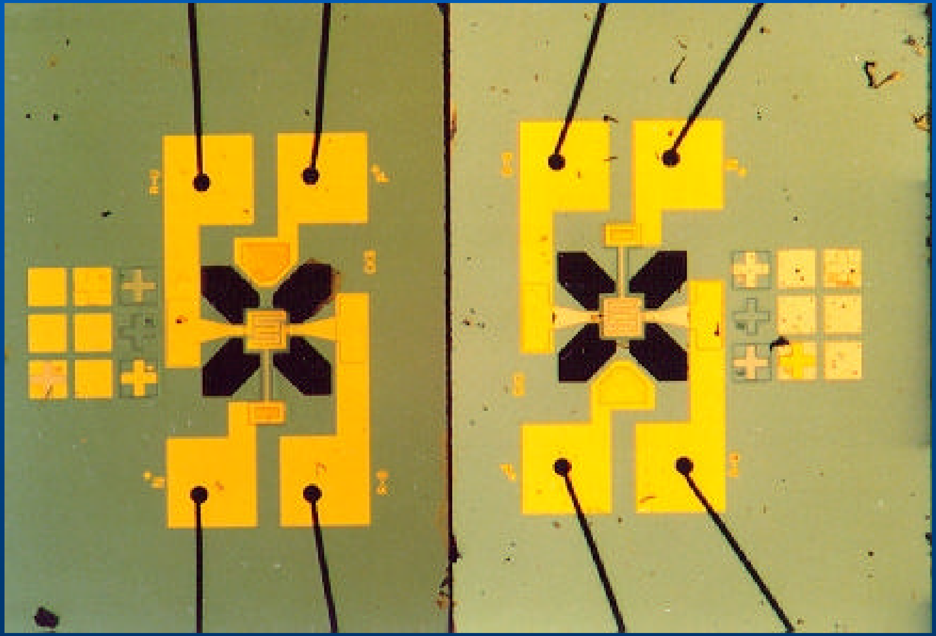
KOH Anisotropic etch

Front side SF_6 plasma etch

Back side SF_6 plasma etch

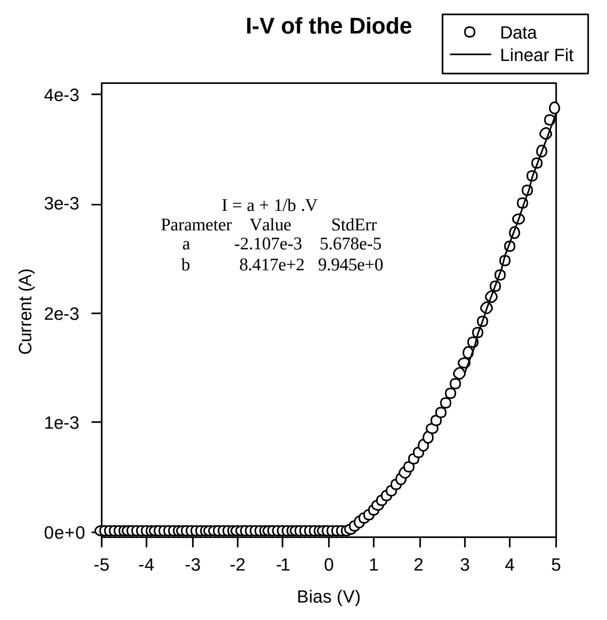
Device Obtained





Device Characterization

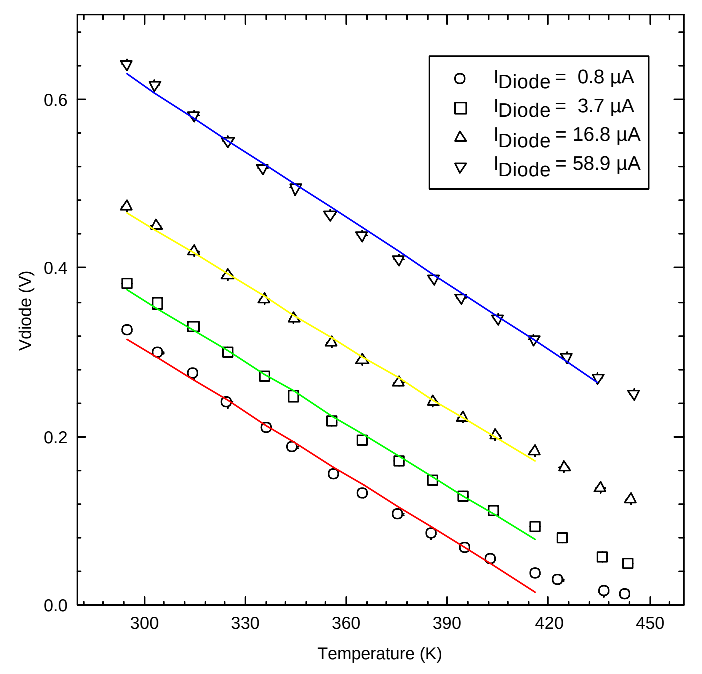
Electrical Characterization



I = a + 1/b .V

Parameter	Value	StdErr
a	-2.107e-3	5.678e-5
b	8.417e+2	9.945e+0

Temperature Calibration

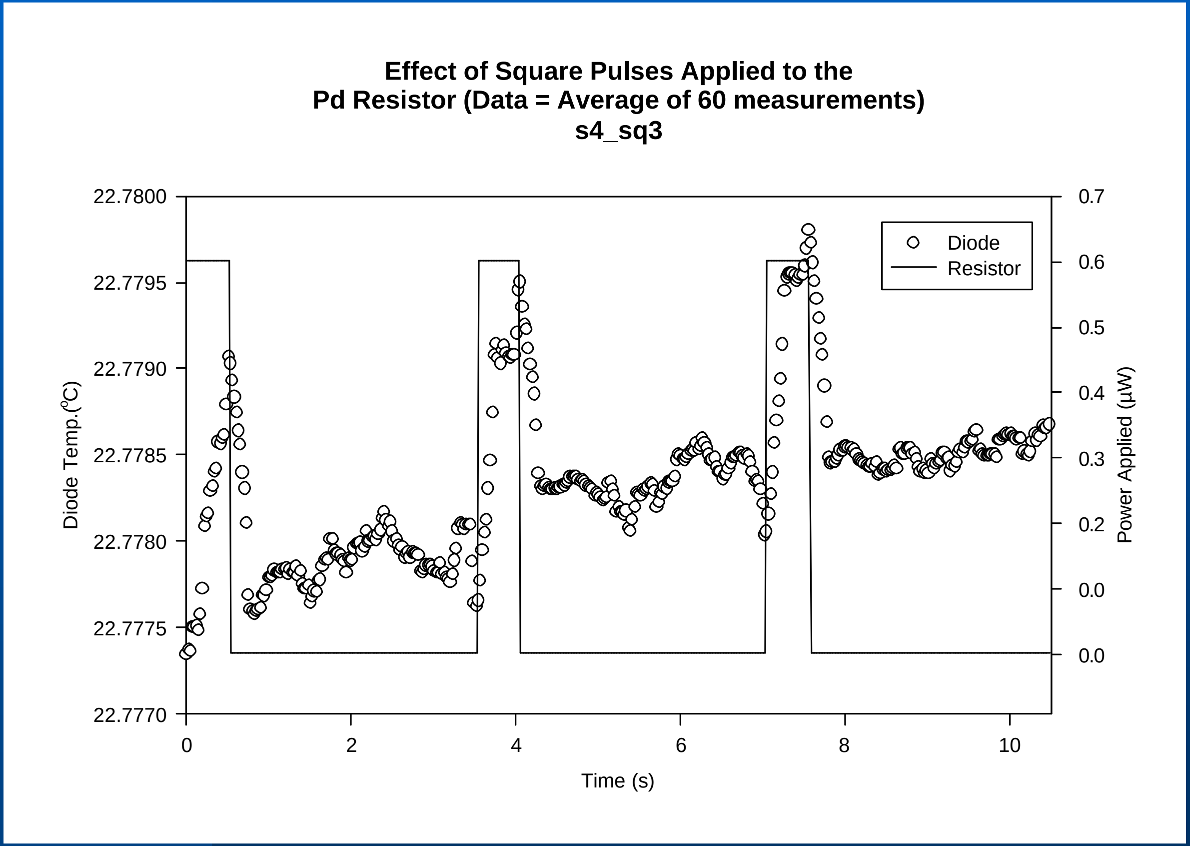


$$I(T) = Ae^{\left(\frac{V_p - E_g}{k_B T}\right)}$$

constant current

$$V_p(T) = \ln\left(\frac{I}{A}\right).k_B T + E_g$$

Thermal behavior under excitation



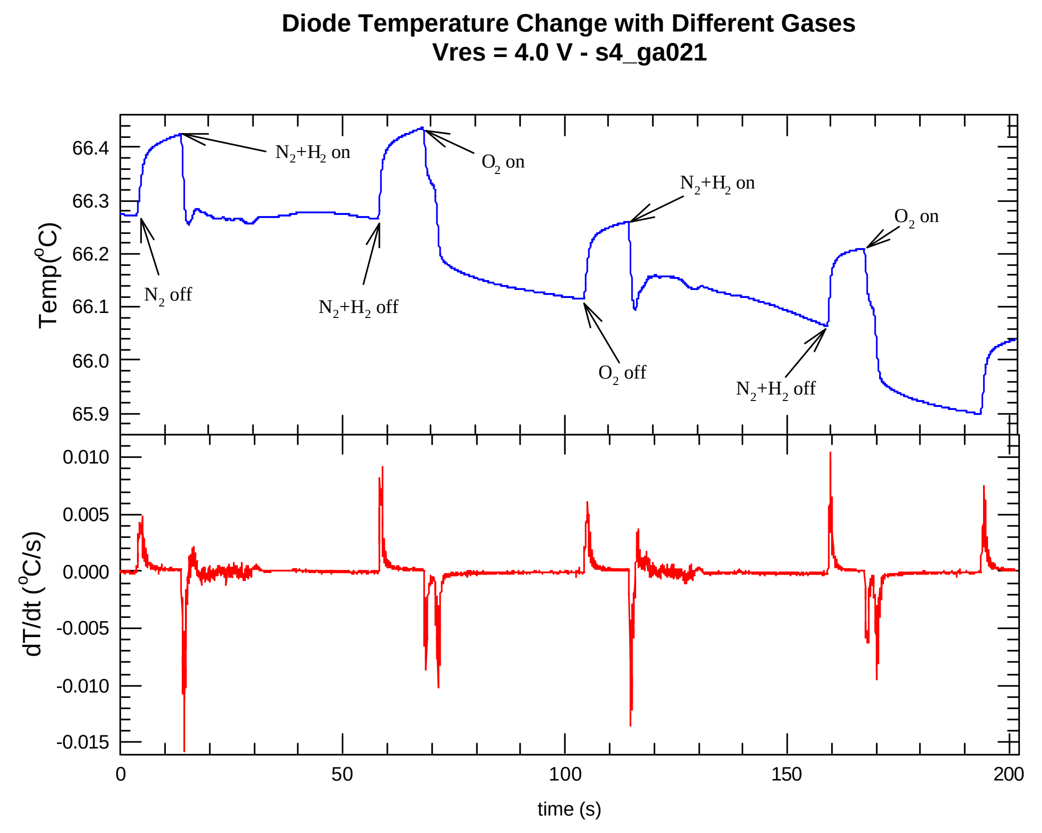
Pulse : 0,6 µW

→ ΔT ~ 1,5 ºC

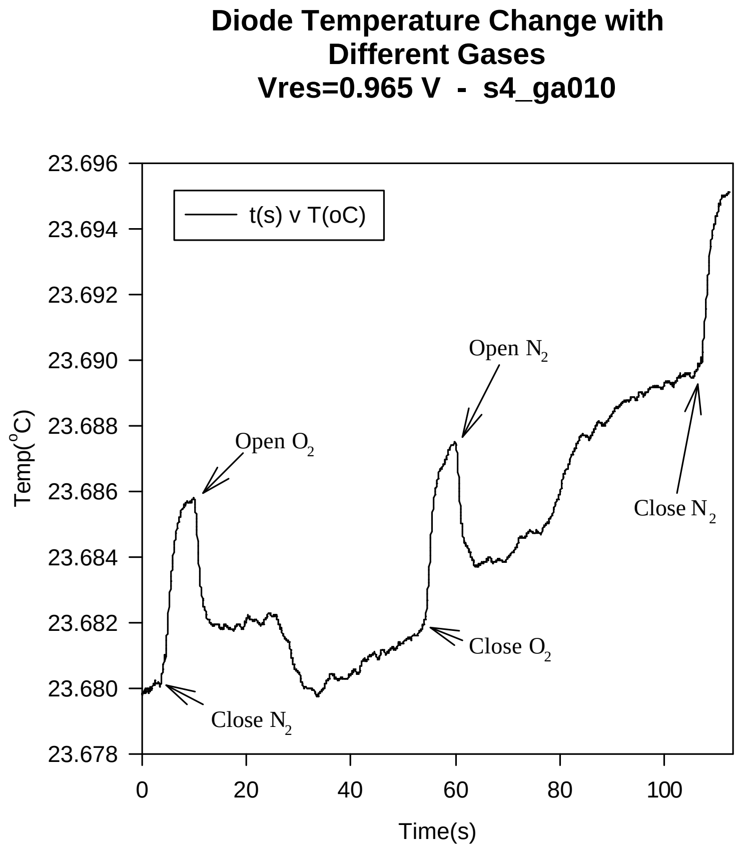
→ Res.: 44µºC

Gas Measurements

Tests for $H_2 + O_2 \rightarrow H_2O$ reaction detection

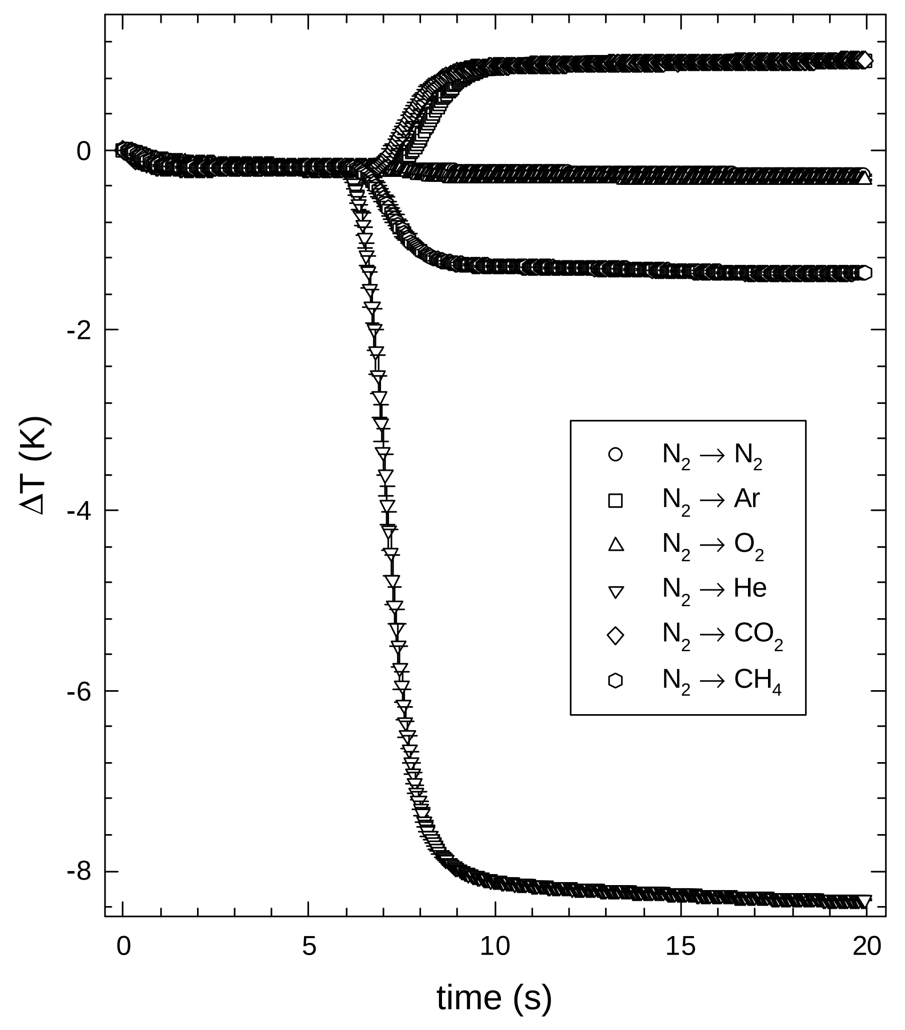


Effects of thermal conductivity detected

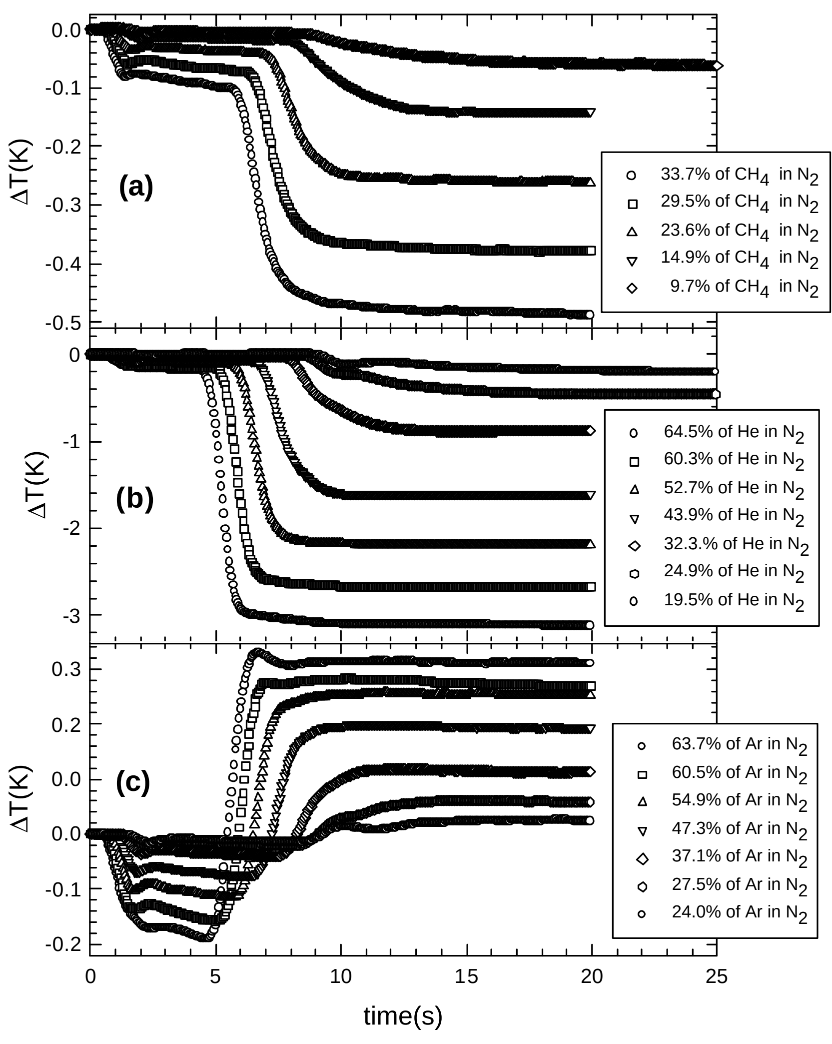


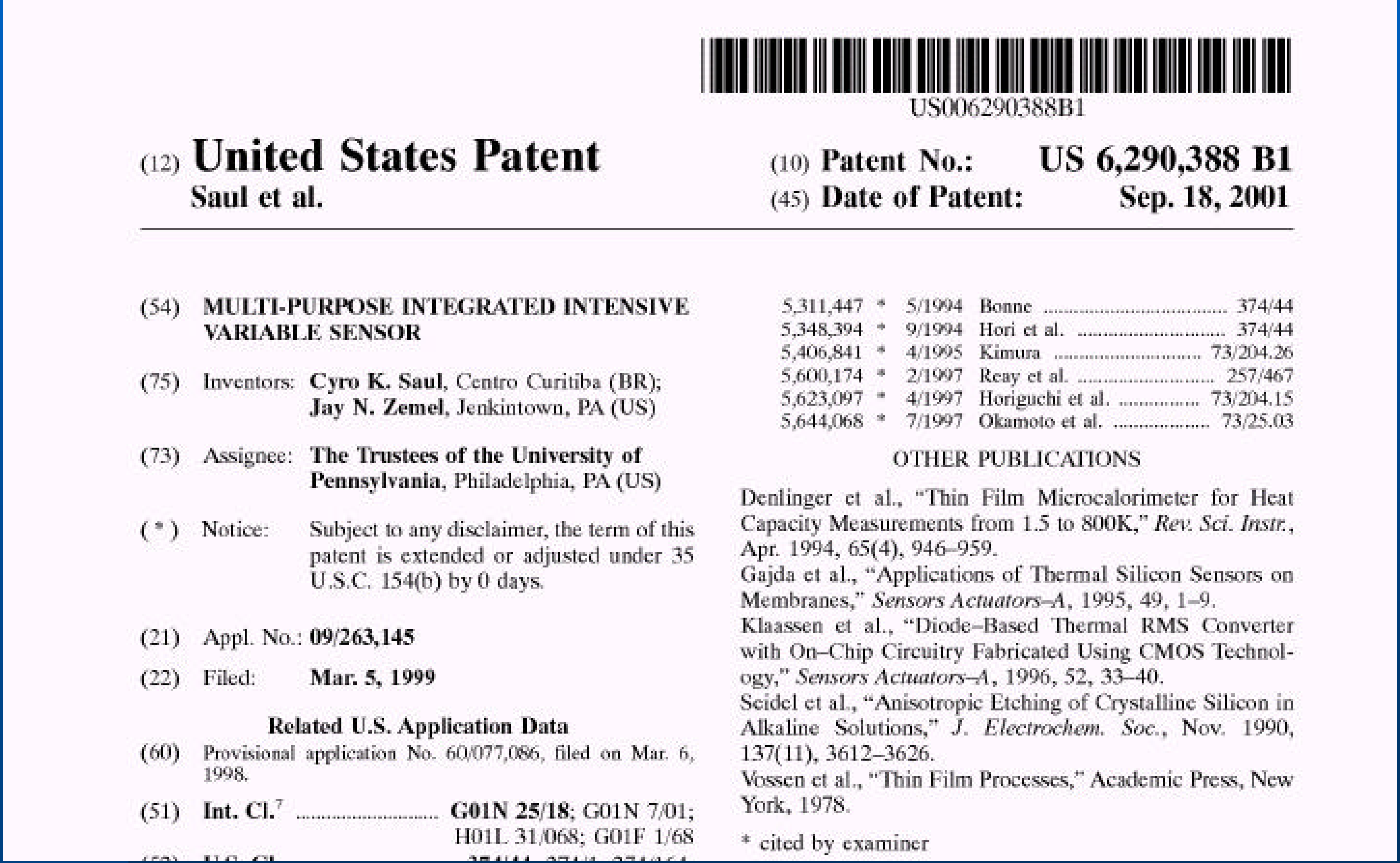
- **Thermal properties**
  - **N_2**
    - **0,02352 W/m^{o}C**
  - **O_2**
    - **0,02396 W/m^{o}C**
  - **$Dk_{N2 ® O2}$ = + 1,87 %**
  - **$Dk_{O2 ® N2}$ = - 1,84 %**

Measurement of pure gases



Measurement of mixed gases





US006290388B1

(12) **United States Patent**
Saul et al.

(10) **Patent No.: US 6,290,388 B1**
(45) **Date of Patent: Sep. 18, 2001**

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(54) **MULTI-PURPOSE INTEGRATED INTENSIVE VARIABLE SENSOR**

(75) Inventors: **Cyro K. Saul**, Centro Curitiba (BR); **Jay N. Zemel**, Jenkintown, PA (US)

(73) Assignee: **The Trustees of the University of Pennsylvania**, Philadelphia, PA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/263,145**

(22) Filed: **Mar. 5, 1999**

Related U.S. Application Data

(60) Provisional application No. 60/077,086, filed on Mar. 6, 1998.

(51) **Int. Cl.**^{7} **G01N 25/18**; G01N 7/01; H01L 31/068; G01F 1/68

5,311,447	*	5/1994	Bonne	374/44
5,348,394	*	9/1994	Hori et al.	374/44
5,406,841	*	4/1995	Kimura	73/204.26
5,600,174	*	2/1997	Reay et al.	257/467
5,623,097	*	4/1997	Horiguchi et al.	73/204.15
5,644,068	*	7/1997	Okamoto et al.	73/25.03

OTHER PUBLICATIONS

Denlinger et al., "Thin Film Microcalorimeter for Heat Capacity Measurements from 1.5 to 800K," *Rev. Sci. Instr.*, Apr. 1994, 65(4), 946–959.

Gajda et al., "Applications of Thermal Silicon Sensors on Membranes," *Sensors Actuators–A*, 1995, 49, 1–9.

Klaassen et al., "Diode–Based Thermal RMS Converter with On–Chip Circuitry Fabricated Using CMOS Technology," *Sensors Actuators–A*, 1996, 52, 33–40.

Seidel et al., "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions," *J. Electrochem. Soc.*, Nov. 1990, 137(11), 3612–3626.

Vossen et al., "Thin Film Processes," Academic Press, New York, 1978.

* cited by examiner

WHEN THE INVENTOR OF THE WHEEL MET THE INVENTOR OF THE DEAL

Main Conclusion

“Microfabrication is the art of learn how <u>not to do</u> each of all steps of the process.”

Acknowledgements

COOPERACION IBEROAMERICANA

CYTED

CIENCIA Y TECNOLOGIA PARA EL DESARROLLO

SUB PROGRAMA IX
Microelectrónica

RED IX.I: TESEO
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