Index

• System Integration

MST: generically related System Integration

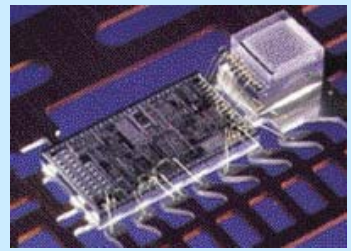
- Microsystems are based on IC technologies
- Fast, high sensibility, cheap, small size, low weight and power consumption.
- Circuits: offsets, temperature, non-linearities compensations and calibration, amplification and autotest functions (Memories and microprocessor)

Type:

Combination of Technologies

- **Hybrid (SoP)**:
  - Wire bonding
  - Multichip substrates (MCM)

- **Simple**
- **Lower development cost**

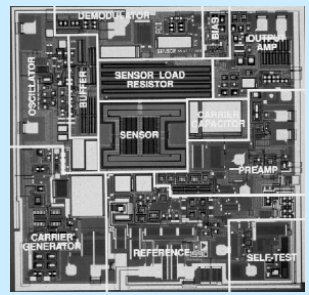


PRESSURE SENSOR
SENSONOR

- **Monolithic (SoC):**
  - IC before MEMS: cheaper (DMD, Texas instrument)
  - Mix fabrication process: (ADXL, Analog devices)
  - MEMS after IC: (iMEMS, Sandia National Laboratories)

  - Surface Micromachining
  - Bulk Micromachining

- **Higher performance**
- **Difficult**
- **Higher development cost**



ADXL50 ANALOG DEVICES

• Monolithic Integration "System on a Chip" (SoC)

The International Technology Roadmap for Semiconductors, ITRS 1999-2001.

- ***System-on-Chip***
  - Trend of IC
  - Cost/performance

IRTS 1999

Cost of adding technology in units of mask levels	Logic	SRAM	Flash	DRAM	CMOS RF	FPGA	MEMS	FRAM	Chemical Sensors	Electro Optical
Logic	0									
SRAM	1–2	0								
Flash	4	3–4	0							
DRAM	4–5	3–4	7–9	0						
CMOS RF	3–5	5–9	6–9	6–10	0					
FPGA	2	2–4	4–6	3–7	5–7	0				
MEMS	2–10	3–12	6–14	6–15	5–15	4–12	0			
FRAM	4–5	3–4	7–9	2–3	7–10	6–7	9–15	0		
Chemical Sensors	2–6	3–7	6–10	6–11	5–11	4–8	4–16	6–11	0	
Electro-Optical	5–8	6–9	9–12	9–13	8–12	7–10	7–18	9–13	7–14	0

ADDED COMPLEXITY IN TERMS OF ADDITIONAL PHOTOLITHOGRAPHIC STEPS

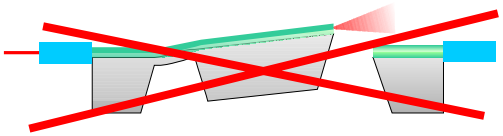
- Add additional technological steps without decrease the CMOS performance

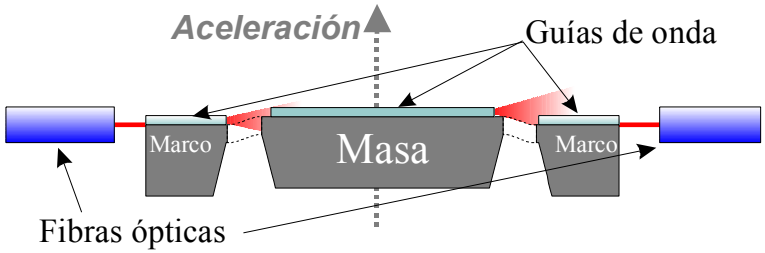
- ***Microsystems***
  - Very different technologies, high complexity of integration.
  - The complexity largely increases with the combination of more than two technologies
  - Couple simulations tools

• Optical Accelerometer

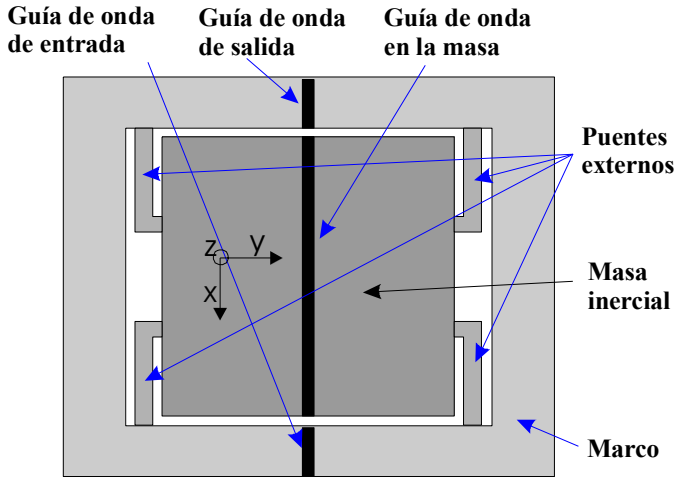
• Idea

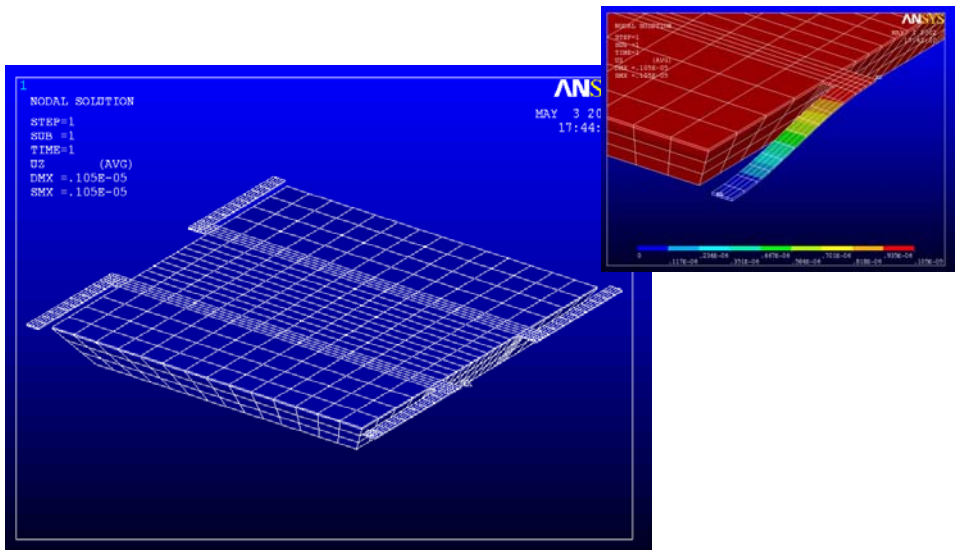
- Free stress structures for an optical accelerometer





• Design





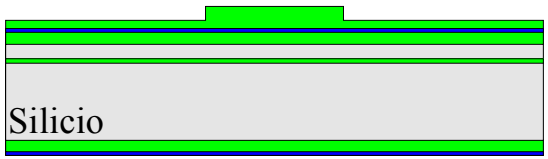
FEM Simulation

Photograph of the optical accelerometer

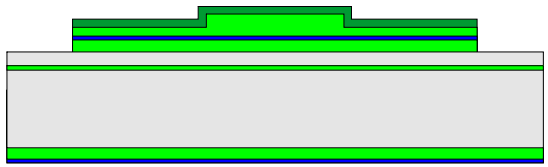
Example 3: Monolithic Integration (Accelerometer+Optic)

- **Technology**
  - BESOI based technology (2+2+1 masks)
  - Arrow waveguides + mechanical structure

Waveguides fabrication



Cross section confinement

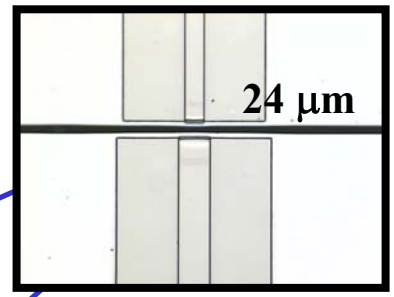


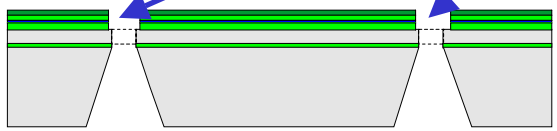
Horizontally confinement of the waveguides

Mechanical structure fabrication

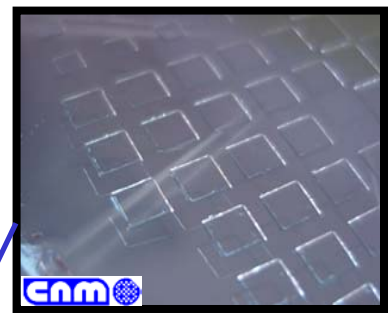
Masks for the anisotropic etching

Anisotropic etching

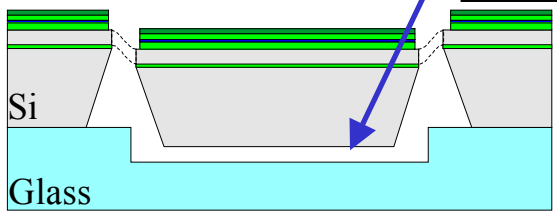




Dry etching



GLASS WAFER

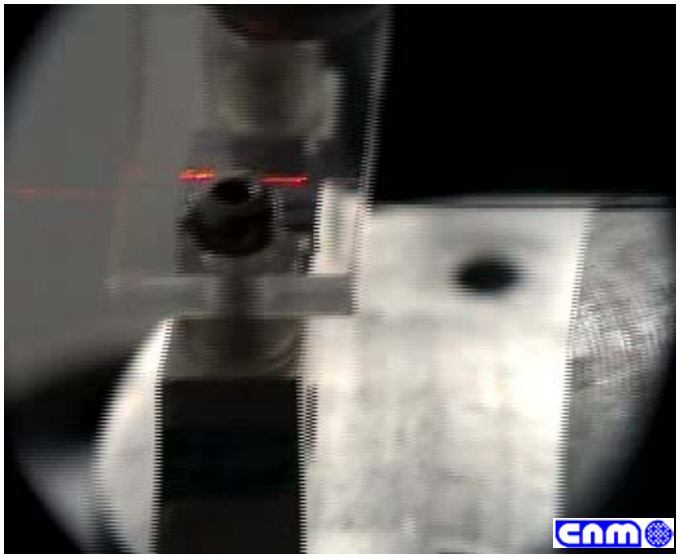


Anodic Bonding

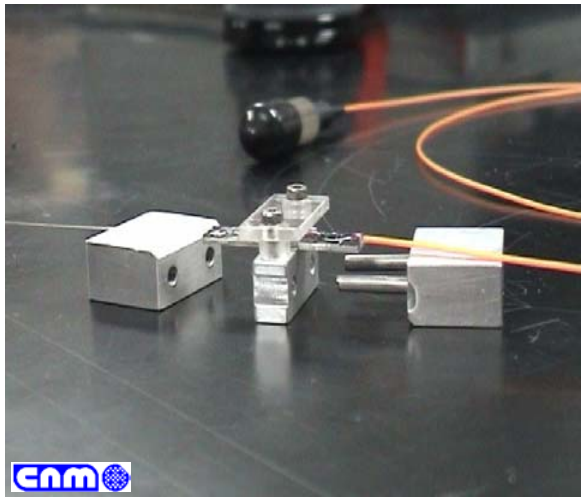
•System Integration

Example 3: Monolithic Integration (Accelerometer+Optic)

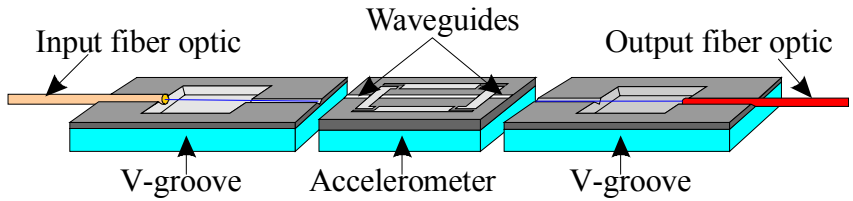
Packaging and Characterisation



PRELIMINARY CHARACTERISATION OF THE OPTICAL ACCELEROMETER

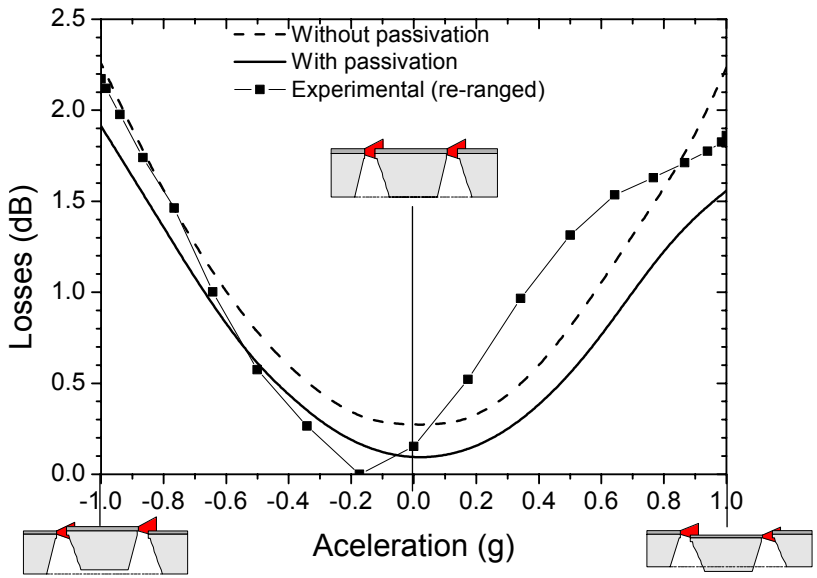


PHOTOGRAPH OF THE PACKAGED DEVICE



SCHEMATIC DRAWING OF AN ACCELEROMETER AND ITS V-GROOVES

Static Characterisation



• Commercialisation Microsystems+IC:

- Microsystems: Small market
- Microsystems companies haven´t IC facilities (Hybrid)
- Companies with IC facilities No MST experience (Monolithic)
- Difficult in a single company/more difficult in several companies

Hybrid

- Low initial cost
- Faster commercialisation
- Easy packaging
- Several systems in a single chip

Small or medium volume of production

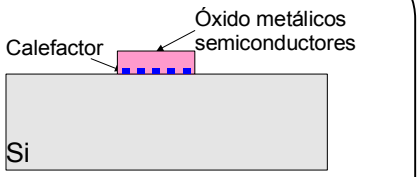
Monolithic

- Smaller and light (cheap)
- Less interconnections and substrates (less fails, cheap)
- Test on wafer (cheap)
- Difficult design and simulation
- Difficult packaging
- Yield!!!

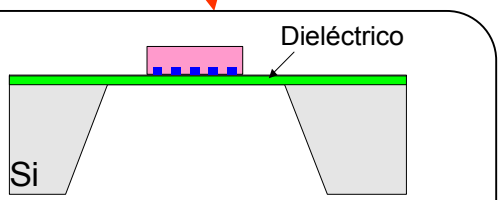
Large volume of production or high added value products

Example 4: Monolithic Integration (Gas sensor+Electronics)

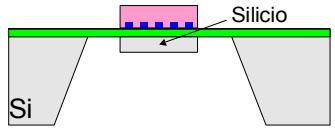
- **Idea**
  - Semiconductors metal oxides change their conductivity in the presence of reactive gases
  - Thick film: high power consumption and expensive interconnections
  - Integration in MST technologies



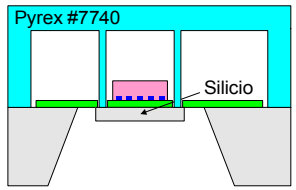
- > 300ºC
- High power consumption



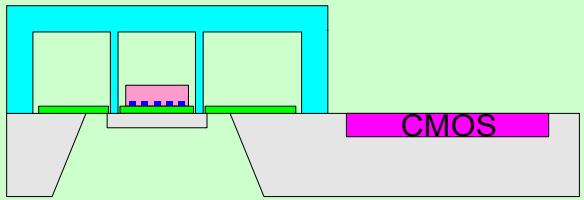
- Dielectric membrane
- Low power consumption
- Bad temperature distribution
- Not robust



- Silicon platform
- Uniform temperature
- Not robust



- Glass, mechanical support
- Pyrex #7740- Hoya SD-2 low thermal conductivity
- Low power consumption



- **CMOS smart sensor**
- Signal processing
- Working temperature control

Applications:

Fire detection

Cabin air quality

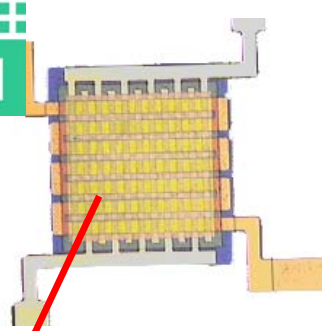
- **GLASGAS-I:** *"A novel methology for manufacturability of robust semiconductor gas sensor arrays"*, UE,ESPRIT III
- **GLASSGAS-II:** *"Silicon/Glass microstructures for innovative gas sensing systems"*, UE, IST-FET-V PM

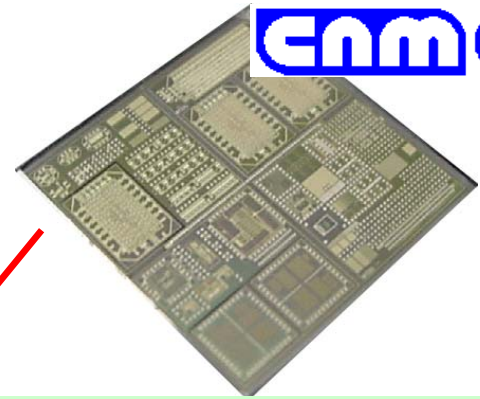
Example 4: Monolithic Integration (Gas sensor+Electronics)

- **Monolithic integration of 3 technologies**

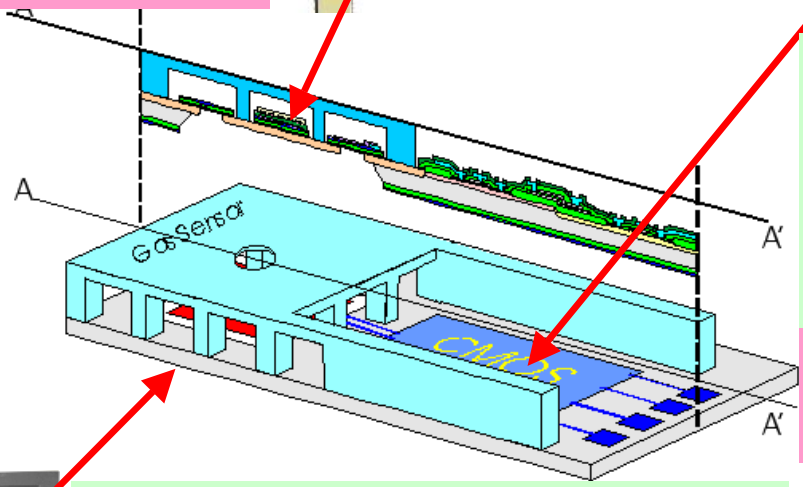
IPM

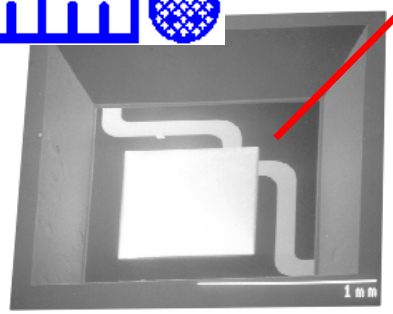
- Pt electrodes
- 4 sensing layers: semiconductor metallic oxides
- **5 masks**
- Low temperature annealing





- CMOS25
- 2 polysilicon levels
- 1-2 metal levels
- **8 masks (1 metal)**
- **10 masks (2 metal)**
- Avoid changes on the CMOS
- Thermal steps before CMOS





- Bulk Micromachining
- Dielectric membrane
- Silicon platform
- High dope layer (etching-stop)
- Pt heater
- Interlevel oxide
- **6 Mask**

EADS CAPTEUR

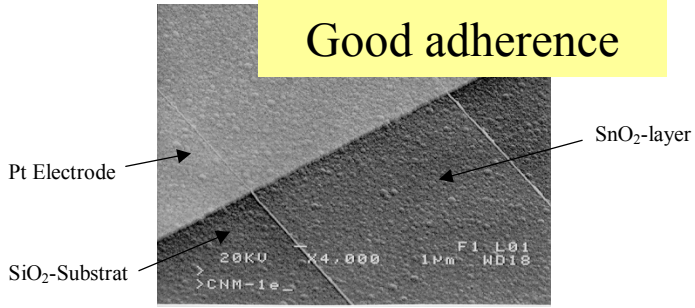
•System Integration

Example 4: Monolithic Integration (Gas sensor+Electronics)

• Compatibility between the technologies

- **Adherence test of platinum and SnO_2 layers**
  - Pt and SnO_2 (IPM)
  - Dielectric layers of the CNM-CMOS : SiO_2 thermal, SiO_2 BPSG, Si_3N_4.

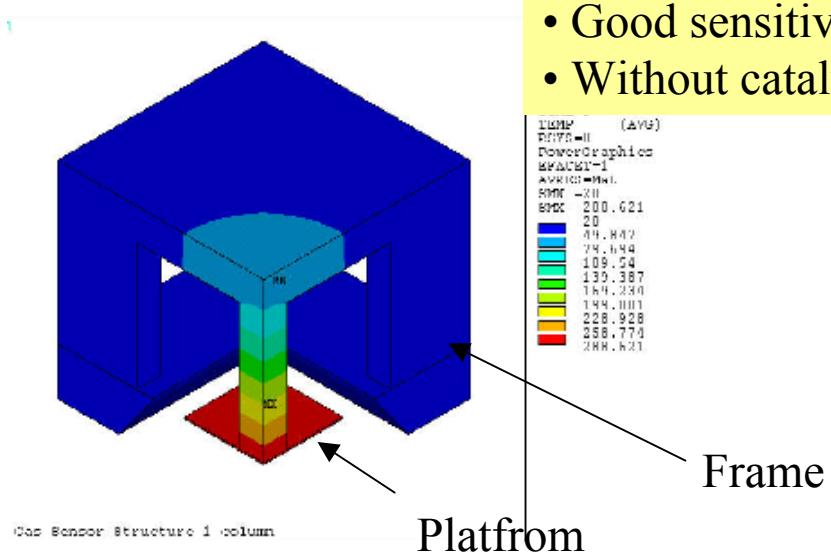
Good adherence

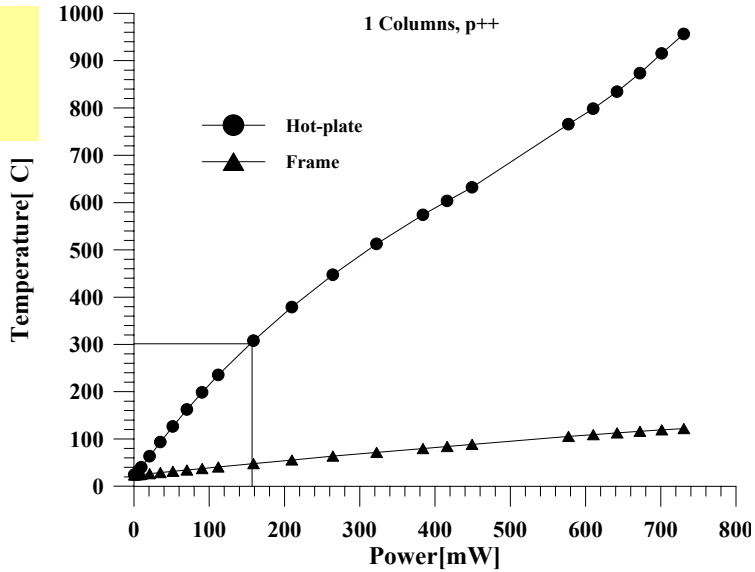


IPM, Freiburg

- **Sensitivity test SnO_2**
  - Standard 700ºC annealing at IPM (Pt catalyser.)
  - 400ºC (Without catalyser, good sensitivity)
  - On-chip annealing (Catalyser)

- Good sensitivity
- Without catalyser

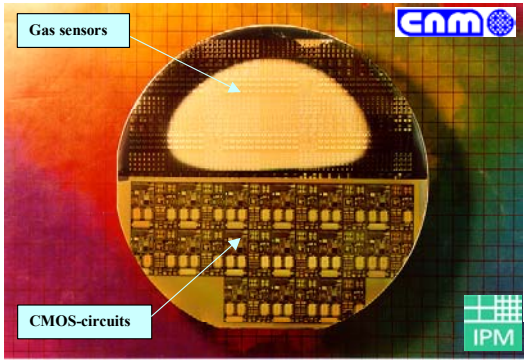




•System Integration

Example 4: Monolithic Integration (Gas sensor+Electronics)

- **Compatibility test CMOS(CNM) + gas sensors (IPM)**



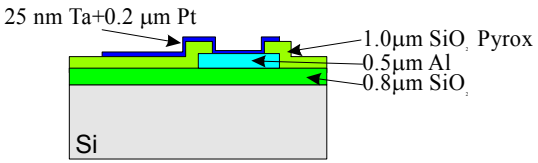
1.- CMOS Technology: test structures
2.- Post-processing: gas sensors

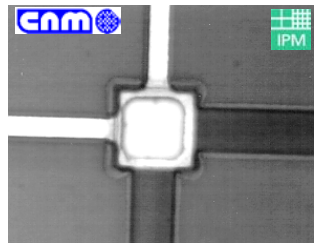
Annealing 400ºC/24h

- CMOS parameters inside the technolgy limits
- Gas sensors with high sensitivity.

- **Contact resistance Al-Pt**

1.- CMOS metallization: Aluminium (CNM)
2.- Electrodes and heater: Platinum (IPM)





KELVIN STRUCTURE

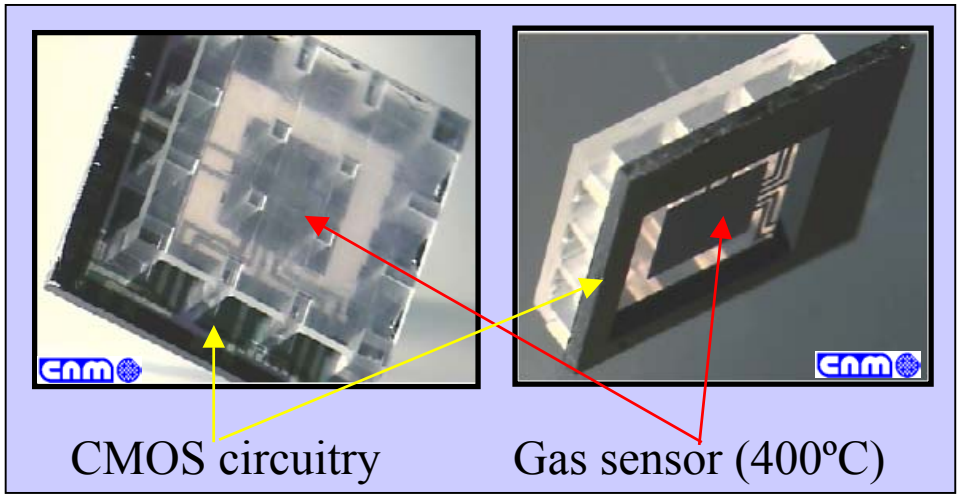
~~• Evaporation~~
- Sputtering

RF cleaning 15min. at 400W

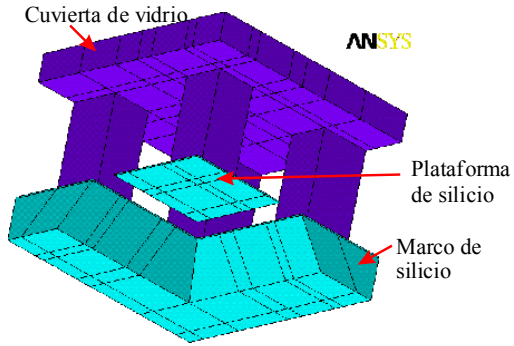
- Aluminium oxide formation during transport
- Pre-cleaning to avoid oxides

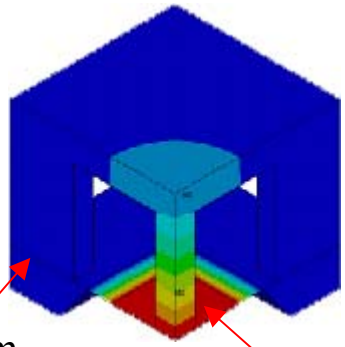
Example 4: Monolithic Integration (Gas sensor+Electronics)

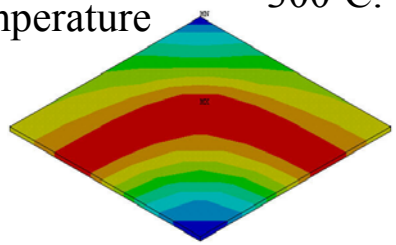
- **Different working temperatures: gas sensor 300-400ºC and CMOS < 80-100ºC**



FEM optimisation of the structure

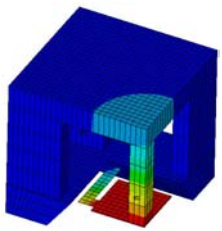


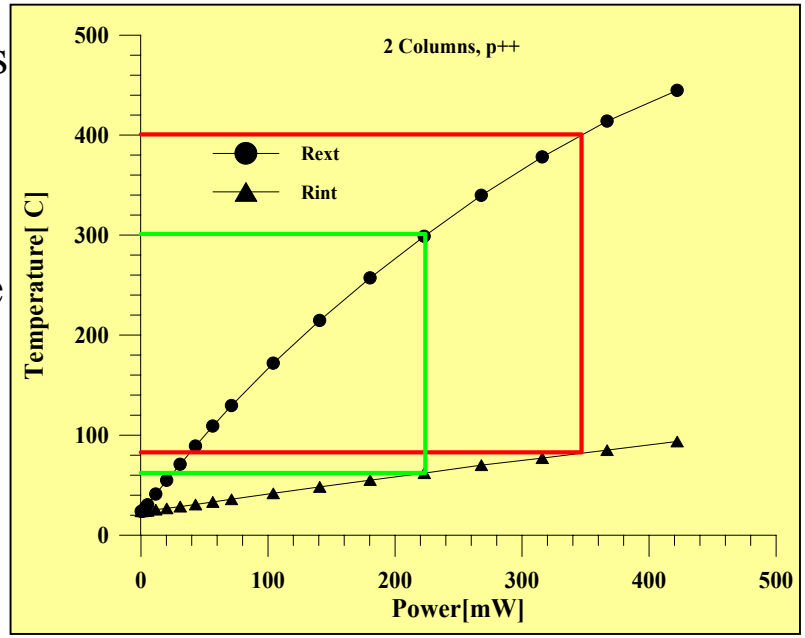




Uniformity <±2ºC

- Glass thickness
- Height of the glass columns
- Width of the glass columns
- Thickness of the platform
- Materials of the membrane
- Thickness of the membrane
- Metal tracks
- Platform-frame distance
- ...





•System Integration

Example 4: Monolithic Integration (Gas sensor+Electronics)

•**Silicon substrates: wafers**

300µm double side polished wafers (fragile)

- Sensor (double side polished wafers and thickness <400µm for double side alignment).
- CMOS (Wafers with p type epitasis on p++ substrates)

Epi-wafers (polish, double side alignment, difficult etch-stop)

- **Silicon nitride membrane for the sensor**

~~• LOCOS silicon nitride of the CMOS~~

~~• PECVD oxinitride of the passivation of the CMOS~~

• LPCVD nitride (good electrical and mechanical characteristics (700ºC: no effect on the CMOS circuitry, deposition before aluminium)

Before aluminium

- **Platinum heater**

At the end of the process

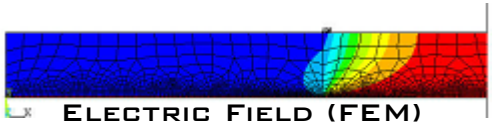
- No CMOS compatible.
- Polysilicon heaters. Low stability. CMOS compatible.

Aging annealing

The nitride membrane has to be deposited before the polysilicon changing the CMOS technology

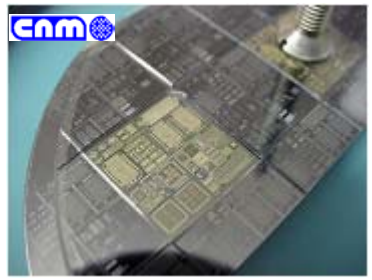
Example 4: Monolithic Integration (Gas sensor+Electronics)

- **Anodic bonding**
  - The high electric field can affect the CMOS circuitries



ELECTRIC FIELD (FEM)

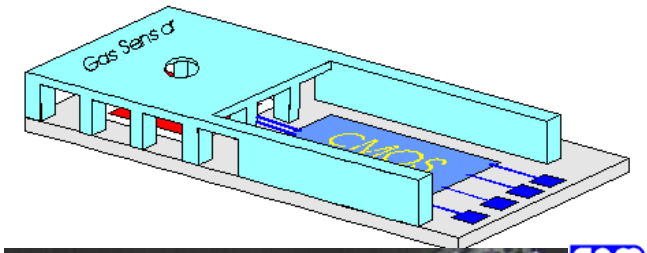
- Capacitors: dielectric breakdown
- Transistors: higher leakage currents

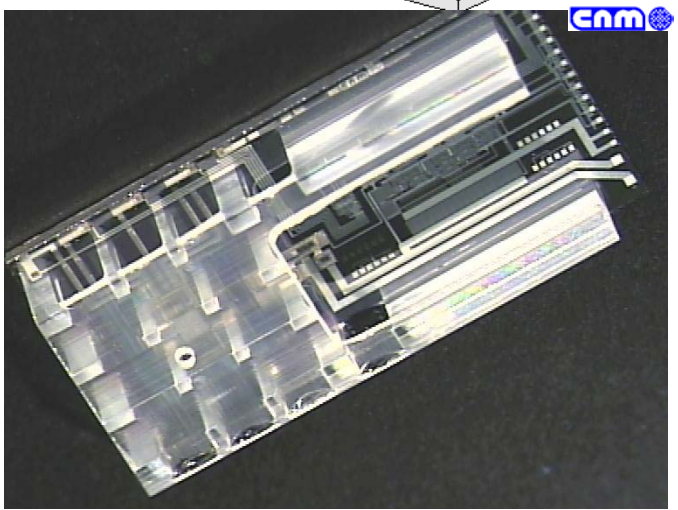


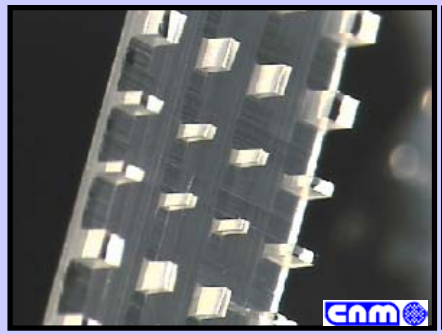
TEST RUN FOR ANODIC BONDING

Allow glass close to circuitries

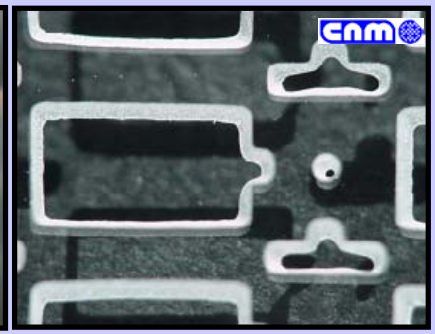
Combination of sawing and sand blasting



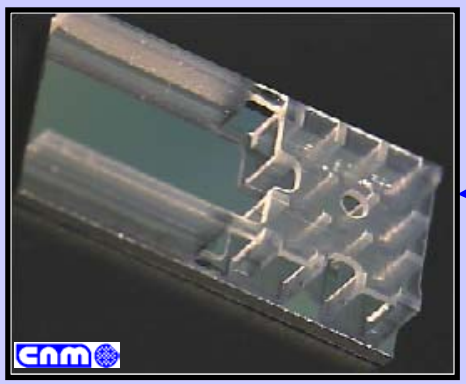




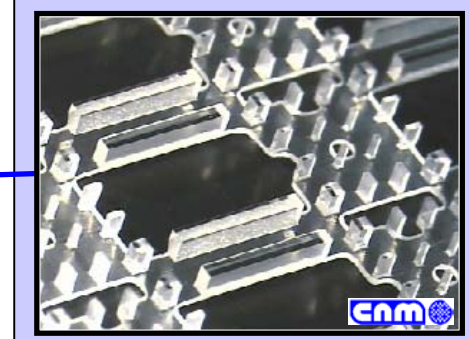
SAWING (COLUMNS)



SAND BLASTING (HOLES)



ANODIC BONDING



COMBINATION OF THE TWO TECHNOLOGIES

Example 4: Monolithic Integration (Gas sensor+Electronics)

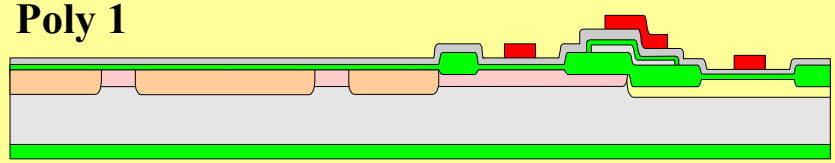
- **Monolithic Integration**

Double side alignment marks

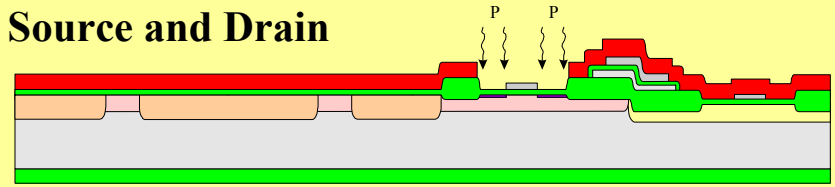
High doped region

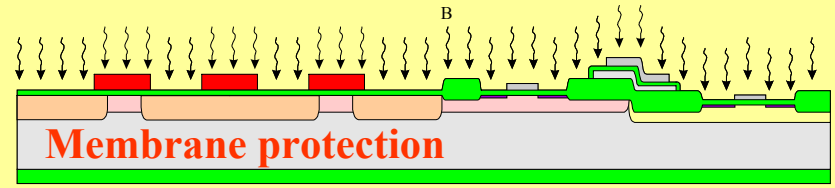
Gas sensor

Poly 1

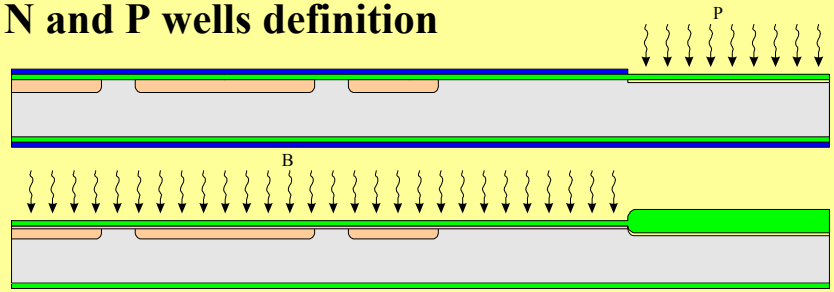


Source and Drain

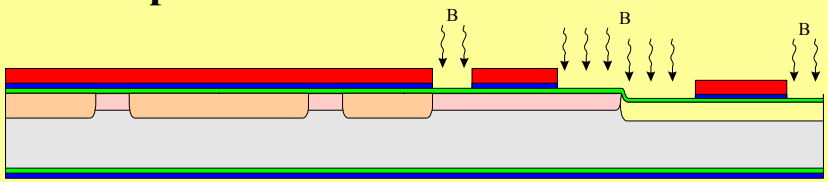




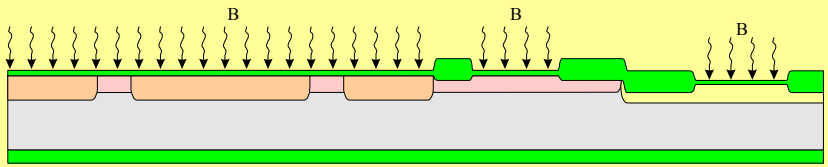
N and P wells definition



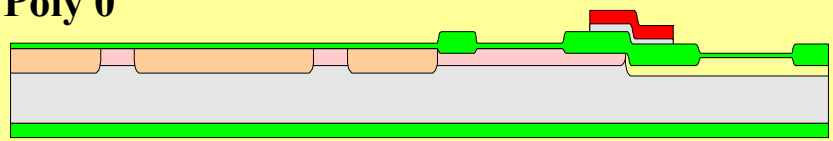
Field implantation: Active areas



Gate implantation

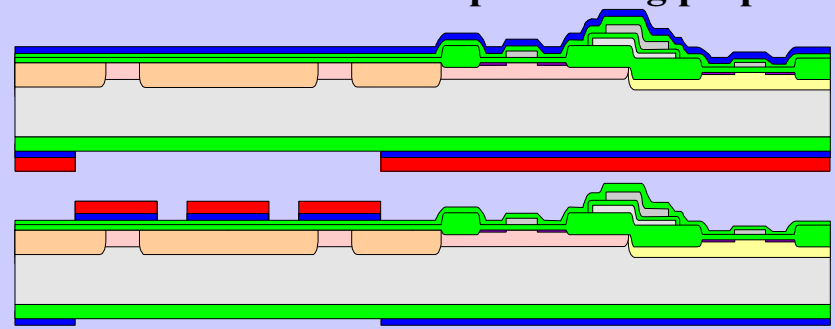


Poly 0

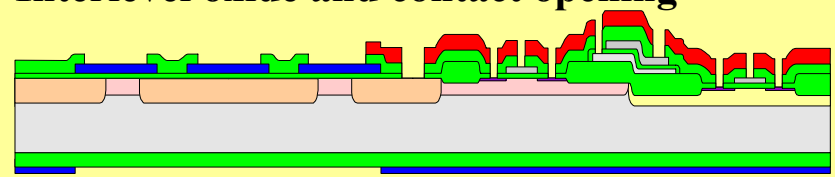


CMOS25

Nit. Membrane-Anisotropic etching prep.



Interlevel oxide and contact opening

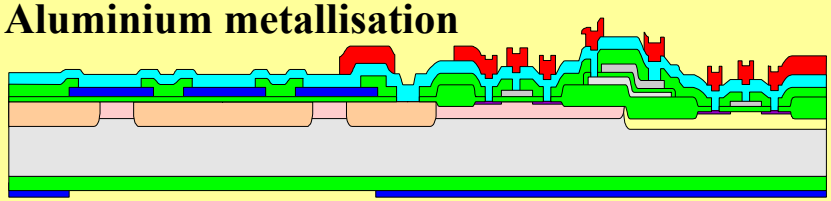


•System Integration

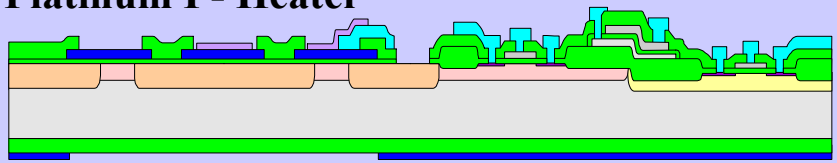
Example 4: Monolithic Integration (Gas sensor+Electronics)

- **Monolithic Integration**

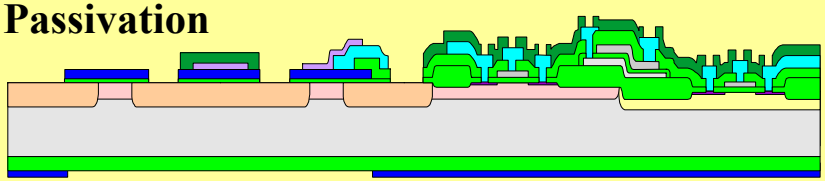
Aluminium metallisation



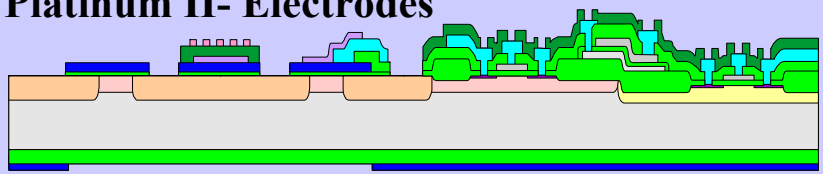
Platinum I - Heater



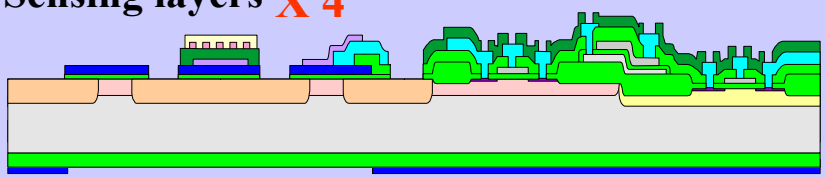
Passivation



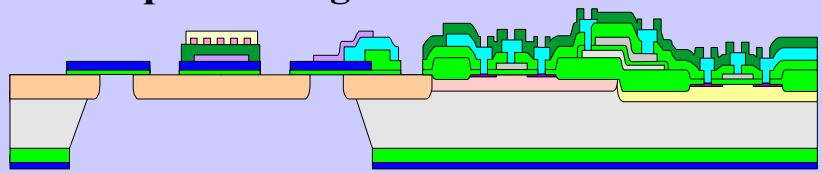
Platinum II- Electrodes



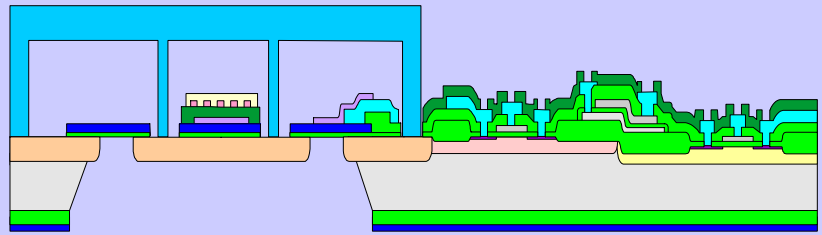
Sensing layers X 4



Anisotropic Etching



Anodic Bonding



Drawbacks

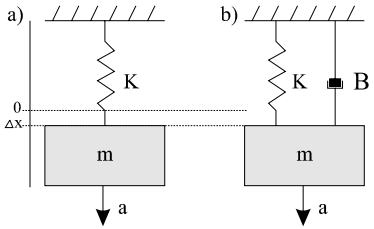
- High technological complexity
- Long and expensive development time
- Low Yield

Advantages

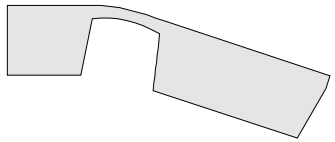
- Small size and weigh, robust
- Less number of interconnections
- Cheap for large volume production

Example 5: Hybrid Integration MCM-D (Accelerometer+Electronics)

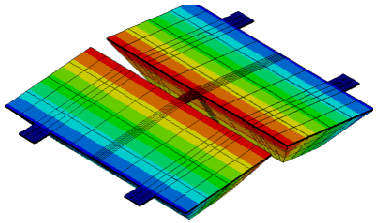
- **Idea**



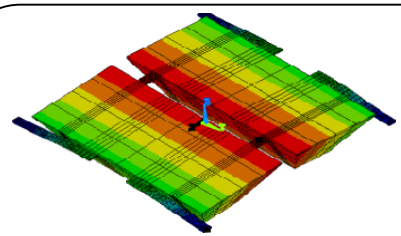
MICROACCELEROMETER



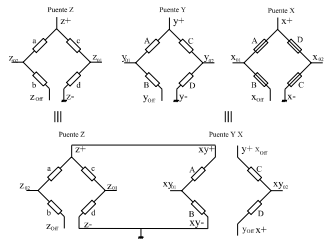
IMPACT TEST



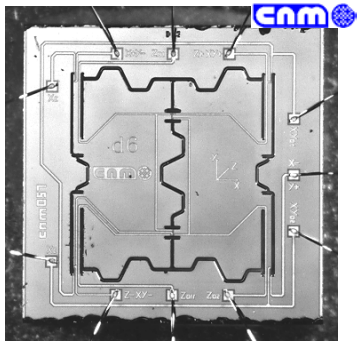
- Twin-mass
- Uniaxial accelerometer

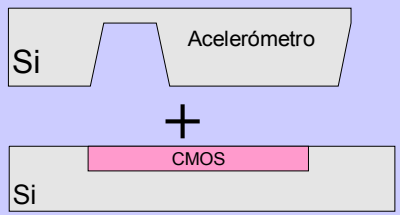


- 6 beams Twin-mass
- Triaxial accelerometer



- Interconnections (1 metal level)
- Low sensitivity





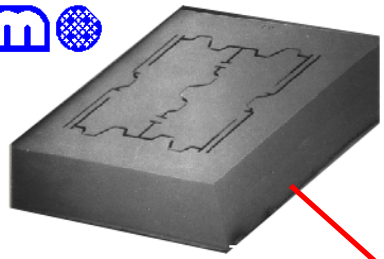
- Circuitry integration
- Several metal levels

•System Integration

• **Encapsulado de microsistemas en formato MCM-D, CICYT**

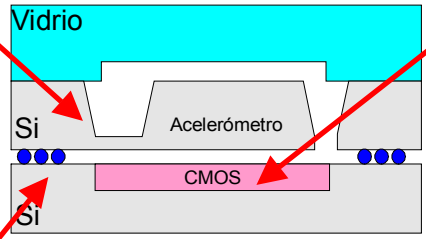
Example 5: Hybrid Integration MCM-D (Accelerometer+Electronics)

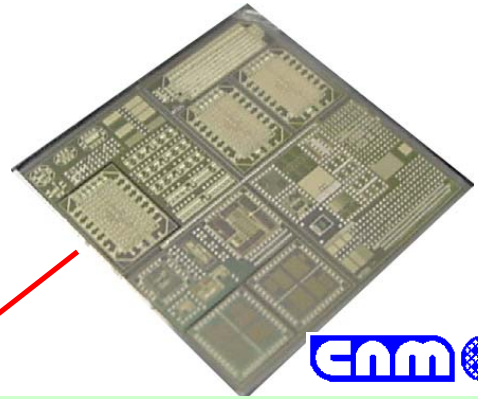
- **Hybrid Integration of 3 technologies**



- BESOI based technology
- Surf. y Bulk Micromachining
- **7 masks**

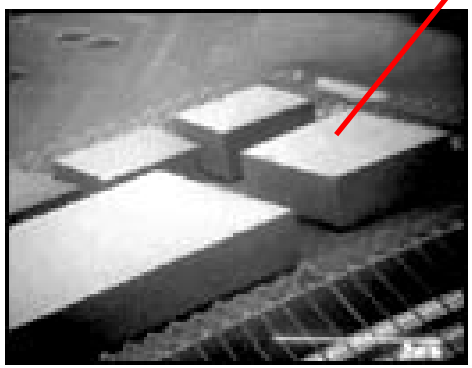
Additional steps:
- passivation
- bondable metallisation





- CMOS25
- 2 polysilicon levels
- 1-2 metals
- **8 masks (1 metal)**
- **10 masks (2 metal)**

CMOS25-CNM technology



- MCM-D technology
- Flip Chip packaging
- 4 metal levels
- Ti+Ni+Au metalisation
- Bonding pads SnPb, SnPbAg
- Silicon substrates (CMOS)
- ***Masks 2x metal level***

Combination with MEMS

Example 5: Hybrid Integration MCM-D (Accelerometer+Electronics)

- **Substrates**
  - Accelerometer sensitive to the packaging stresses
  - CMOS-Silicon substrates.

MCM substrates of silicon

- **Accelerometer metallisation**
  - Aluminium.

- Passivation oxide
- Bondable metallisations

No interference with the accelerometer technology

- **CMOS + MCM metallisation**
  - Aluminium.

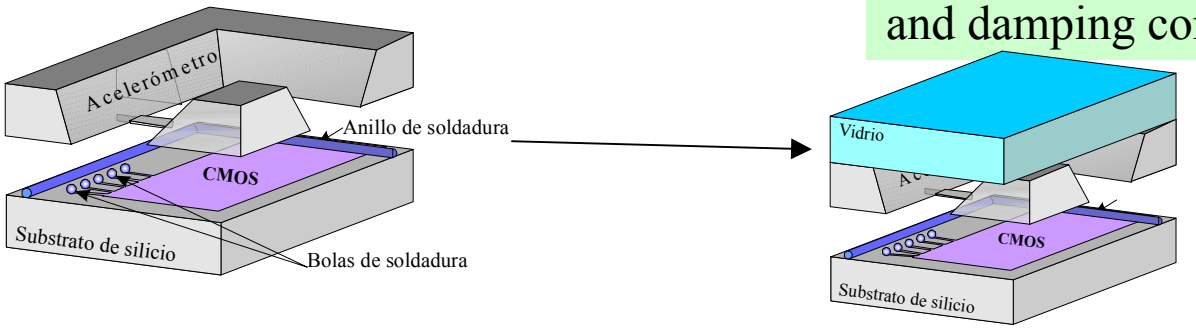
- Polyamide 1, Aluminium 2
- Polyamide 2, Aluminium 3
- Polyamide 3, Bondable metallisation Ni+Ti+Au

Up to 4 levels

Post-processing

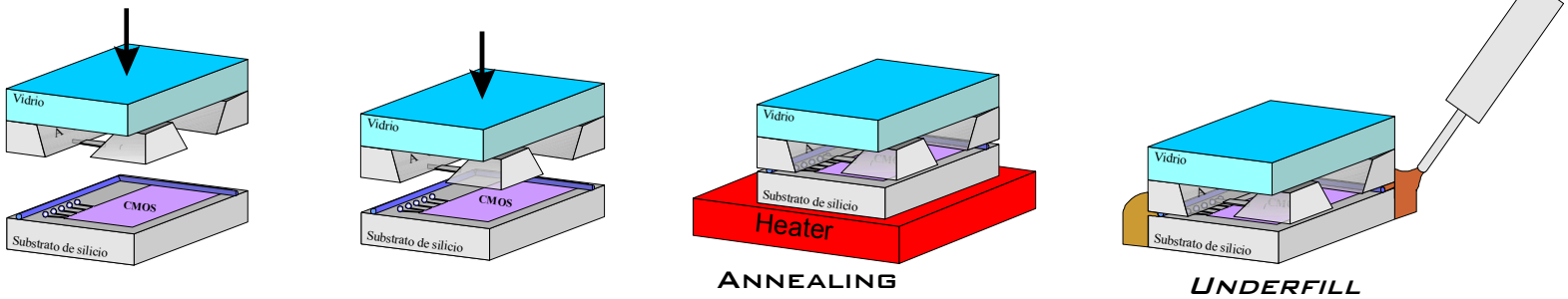
- **Backside protection of the accelerometer during *flip-chip***
  - Anodic bonding of a glass wafer

Glass wafer is used as protection and damping control.

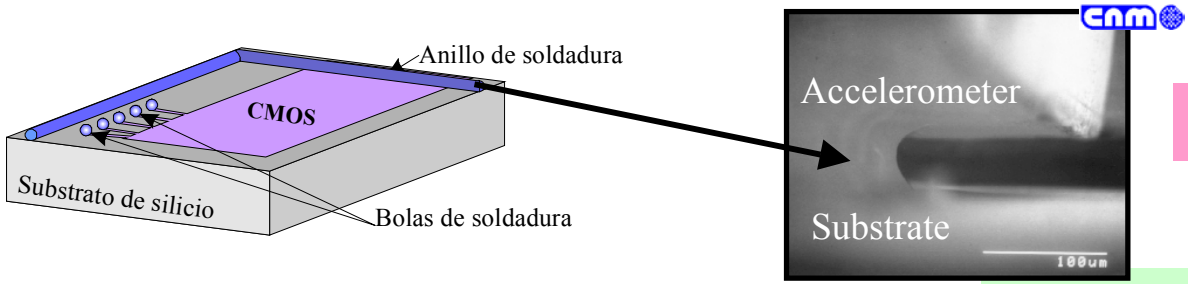


Example 5: Hybrid Integration MCM-D (Accelerometer+Electronics)

- **Sticking problems of the mass during reflow**



The protective silicone can stick the mass.



Ring of bonding paste

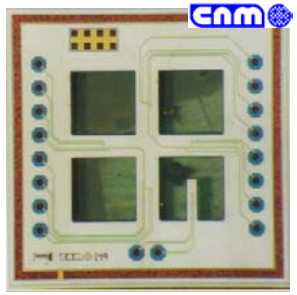
No additional technological steps

- **Annealing of the bumps**

Low temperature <220ºC No effects on CMOS/Acelerometer

- **Stresses due to the flip-chip process**
  - Silicon substrate
  - Bumps and bonding ring

Low temperature



DADO DE TEST

Example 5: Hybrid Integration MCM-D (Accelerometer+Electronics)

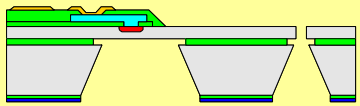
- Hybrid Integration process

Anisotropic etching preparation

Piezoresistor definition and metalisation

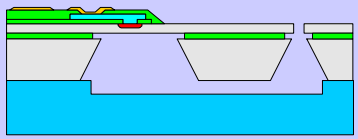
Accelerometer

Passivation and bondable metallisation



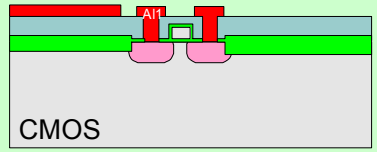
MCM

Anisotropic etching, RIE and anodic bonding



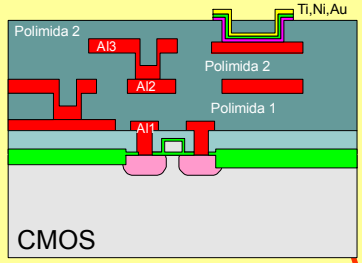
Accelerometer

CMOS25

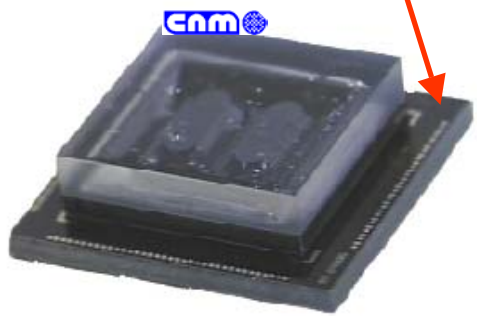


CMOS

Polyamide, Aluminium and Gold



MCM



Advantages

- Small initial cost of development
- Faster commercialisation
- Easier packaging
- Several Microsystems in the same chip

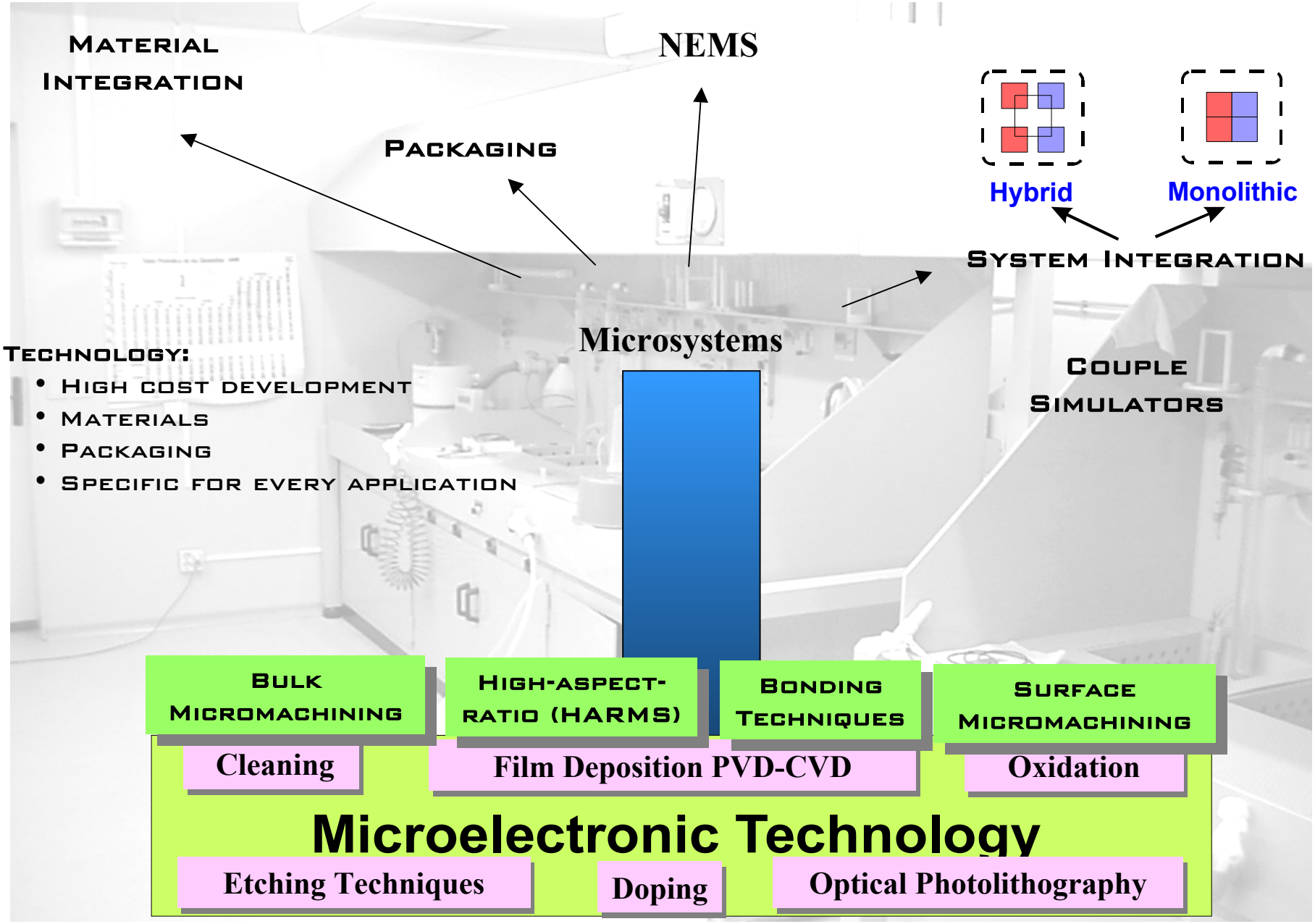
Drawbacks

- Flip-chip high cost

$$Coste_{MEMS} = f(C_{desarrollo} + C_{producción})$$

Small/medium volume production

•System Integration


Material Integration
NEMS
Packaging
Hybrid
Monolithic
System Integration
Microsystems
Technology:
• High cost development
• Materials
• Packaging
• Specific for every application
Couple Simulators
Bulk Micromachining
High-aspect-ratio (HARMS)
Bonding Techniques
Surface Micromachining
Cleaning
Film Deposition PVD-CVD
Oxidation
Microelectronic Technology
Etching Techniques
Doping
Optical Photolithography

Muchas gracias
por su atención

Obrigado pela
sua atenção